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DEFENCE RESEARCH ESTABLISHMENT OTTAWA
REPORT NO. 1279

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Abstract

EHF SATCOM offers communications robustness by incorporating wide-band frequency-hopping and on-board satellite processing to mitigate the effects of electronic interference. The same characteristics that make EHF SATCOM robust however, also make it complex. Satellite on-board processing means that synchronization must be achieved for both the uplink and the downlink. The Skynet EHF (extremely high frequency) Downlink Trials consisted of several week-long accesses over Skynet 4A during 1993 and 1994. The whole link (up to satellite and back down) was used to simulate an EHF frequency-hopped downlink from a processing satellite.

To aid in the analysis of EHF SATCOM, in-house ground terminal and payload simulators were developed. For this set of trials, the synchronization and communications aspects of an EHF frequency-hopped downlink using burst differential phase-shift keying modulation were investigated. The payload and ground terminal simulators were developed using a combination of off-the-shelf components and in-house developed hardware and software. The implementation of these two simulators is detailed in this report after the description of the experimental waveform.

The Skynet EHF Downlink Trials were successfully run in week-long experiments over two years. Frequency-hopped spatial and time synchronization were achieved. Data and voice communications were demonstrated with and without time diversity. Problems with the commercial frequency hopping synthesizers precluded the completion of some of the data communications experiments in the time available.

Résumé

La communication par satellite dans la bande millimétrique (EHF) est rendue plus robuste contre le brouillage électronique en utilisant les sauts de fréquence et le traitement numérique des signaux dans la charge utile. Les caractéristiques qui rendent cette communication robuste la rendent aussi plus complexe parce qu'il faut faire la synchronisation des liaisons montantes et descendantes. Les essais Skynet de liaison satellite-terre à EHF, consistant en des accès d'une durée d'une semaine à la fois, se sont déroulés en 1993 et 1994. La liaison unidirectionnelle totale (de station terrestre à Skynet à station terrestre) est utilisée pour simuler un liaison descendante d'un satellite EHF avec traitement numérique des signaux.

Pour la recherche des aspects de communication par satellite à EHF, des simulateurs de station terrestre et de charge utile ont été développés. La synchronisation et la communication de données par rafales de transmission de signaux modulés par déplacement de phase différentiel (DPSK) d'une liaison descendante d'un système EHF utilisant les sauts de fréquence ont été étudiées pendant ces essais. Les simulateurs ont été construits en se servant d'une combinaison de matériel et de logiciel existants et développés par le CRDO (Centre de recherches pour la défense, Ottawa). Les détails des simulateurs et des signaux sont donnés dans ce rapport.

La synchronisation temporelle et spatiale de la liaison satellite-terre ont été obtenue. Les communications numériques des données et de la voix ont été démontrées avec ou sans la diversité dans le temps. Les problèmes avec les générateurs de sauts de fréquence commerciaux ont empêchés l'achèvement de toutes les expériences de communication de donnée pendant la période disponible.

Executive Summary

The MILSATCOM Groups at Defence Research Establishment Ottawa (DREO) and Communications Research Centre (CRC) have been involved in the research and development of Extremely High Frequency Satellite Communications (EHF SATCOM) to better assess the associated capabilities, limitations and complexities. EHF SATCOM offers communications robustness by incorporating wide-band frequency-hopping and on-board satellite processing to mitigate the effects of electronic interference. The same characteristics that make EHF SATCOM robust however, also make it complex. Satellite on-board processing means that each ground terminal must achieve synchronization for both the uplink and the downlink. This requirement coupled with the use of frequency-hopping requires the ground terminal to have an agile, wideband frequency synthesis capability for the uplink and downlink. In addition, doppler frequency offsets due to relative motion between the satellite and ground terminal can become significant at EHF, typically requiring frequency offset compensation by the ground terminal.

To aid in the analysis of EHF SATCOM, in-house ground terminal and payload simulators were developed. The simulators were initially developed at nominal uplink and downlink frequencies of 44 GHz and 20 GHz. The use of the Skynet 4A satellite necessitated a change in the nominal simulator uplink and downlink frequency and a reduction in the hopping bandwidth. The nominal uplink and downlink frequencies for the EHF frequency-hopping trials were 44.6 GHz and 7.6 GHz, respectively with a hopping bandwidth of 50 MHz. Since Skynet 4A is an inclined geosynchronous but non-stationary satellite, spatial tracking was required.

For this set of trials, the synchronization and communications aspects of an EHF frequency-hopped downlink using burst differential phase-shift keying modulation were investigated. Downlink synchronization was chosen because it is the first step in overall synchronization. Future experiments will explore uplink synchronization. The whole link (up to satellite and back down) was used to simulate an EHF frequency-hopped downlink from a processing satellite.

The payload and ground terminal simulators were developed using a combination of off-the-shelf components and in-house developed hardware and software. The implementation of these two simulators is detailed in this report after the description of the experimental waveform. Within an appendix, the algorithm used for downlink temporal synchronization is described.

The heart of the payload simulator was the Downlink Waveform Processor which was responsible for generating the appropriate waveform to be transmitted to the Skynet satellite. Since the experiment occurred over a satellite, antennas and controllers were also necessary. The entire payload simulator was located at CRC, split between the transmitter on the roof and the antenna controller in a laboratory.

The ground terminal simulator was installed in a second terminal at DREO. The Synchronization and Timing Controller was the main processor in the ground terminal simulator. There was also an antenna controlling computer, a burst demodulator computer and a data logger to record the results of the experiments.

The Skynet EHF Downlink Trials were successfully run in week-long experiments over two years. Frequency-hopped spatial and time synchronization were achieved. Data and voice communications were demonstrated with and without time diversity. Problems with the commercial

frequency hopping synthesizers precluded the completion of some of the data communications experiments in the time available.

These trials provided the MILSATCOM groups an opportunity to research robust satellite frequency-hopped synchronization and communications. This experience has proven invaluable in the support of the D6470 project, specifically for the EHF system simulator being developed in industry.

Work has already begun for Skynet EHF Uplink Trials to work on the other aspect of system synchronization as well as examining frequency-shift-keying (FSK) modulation for uplink data. Once this work at low-data-rates (LDR) is complete, consideration should be given to future trials at medium data rates (MDR) since the demand for data in the modern military environment is continuously increasing.

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Acknowledgements

The success of the simulator development and of the EHF trials was due to the efforts of a relatively small but dedicated supporting cast including David Barlow, Eric Boudriau, Raymond Burrill, Robert Keightley, Douglas Lambert, Pierre Richer and Lyle Wagner.

The trials could not have occurred without the generous support provided by Defence Research Agency (DRA) in the United Kingdom who provided us with access to the Skynet 4A satellite. Through a TTCP STP-6 agreement, we were able to use extensive time and bandwidth resources of the satellite at no cost for these trials.

The efforts of Gus Williams of DRA, particularly in the provision of satellite orbital elements for each week of the trials, are appreciated.

1 - Introduction

The MILSATCOM groups at Defence Research Establishment Ottawa (DREO) and Communications Research Centre (CRC) have been involved in the research and development of EHF SATCOM to better assess the associated capabilities, limitations and complexities. EHF SATCOM offers communications robustness by incorporating wide-band frequency-hopping and on-board satellite processing to mitigate the effects of electronic interference. The same characteristics that make EHF SATCOM robust however, also make it complex. Satellite on-board processing means that each ground terminal must achieve synchronization for both the uplink and the downlink. This requirement coupled with the use of frequency-hopping requires the ground terminal to have an agile, wideband frequency synthesis capability for the uplink and downlink. In addition, doppler frequency offsets due to relative motion between the satellite and ground terminal can become significant at EHF, typically requiring frequency offset compensation by the ground terminal.

DREO and CRC have been active in the area of EHF SATCOM through numerous in-house studies and hardware/software developments. A significant portion of the in-house effort has been in the area of downlink [1,2] and uplink [3-5] synchronization of frequency-hopped differential phase-shift-keying (FH/DPSK) and frequency-hopped M-ary frequency-shift-keying (FH/MFSK), respectively. Digital demodulation techniques including diversity combining for MFSK [6-9] and multiple-symbol differential detection of DPSK [10,11] have also been investigated. [12] documents the development and control of agile frequency synthesizers whereas [13,14] cover multi-beam antennas. DREO has been active in the development in industry of an EHF testbed (D6470) conforming to the US MIL-STD-1582.

To aid in the analysis of EHF SATCOM, in-house ground terminal and payload simulators were developed. The simulators were initially developed at nominal uplink and downlink frequencies of 44 and 20 GHz. EHF frequency-hopping trials over the Skynet 4A satellite using these simulators, located at different antennas approximately 1 km apart, were proposed in mid-92 and discussed in [15,16]. The use of the Skynet 4A satellite necessitated a change in the nominal simulator uplink and downlink frequency and a reduction in the hopping bandwidth. The nominal uplink and downlink frequencies used for the EHF frequency-hopping trials were 44.6 GHz and 7.6 GHz, respectively with a hopping bandwidth of 50 MHz. Since Skynet 4A is an inclined geosynchronous but non-stationary satellite, spatial tracking was required.

For this set of trials, the synchronization and communications aspects of an EHF FH/DPSK downlink were investigated. That is, the link under investigation is from the payload simulator to the ground terminal simulator via Skynet 4A, as shown in Fig. 1. The whole link (up to satellite and back down) was used to simulate an EHF frequency-hopped downlink from a processing satellite. Since Skynet 4A is a transponding satellite, only one link (uplink or downlink) could be investigated at a time. Downlink synchronization was chosen because it is the first step in overall synchronization. Future experiments will explore uplink synchronization.

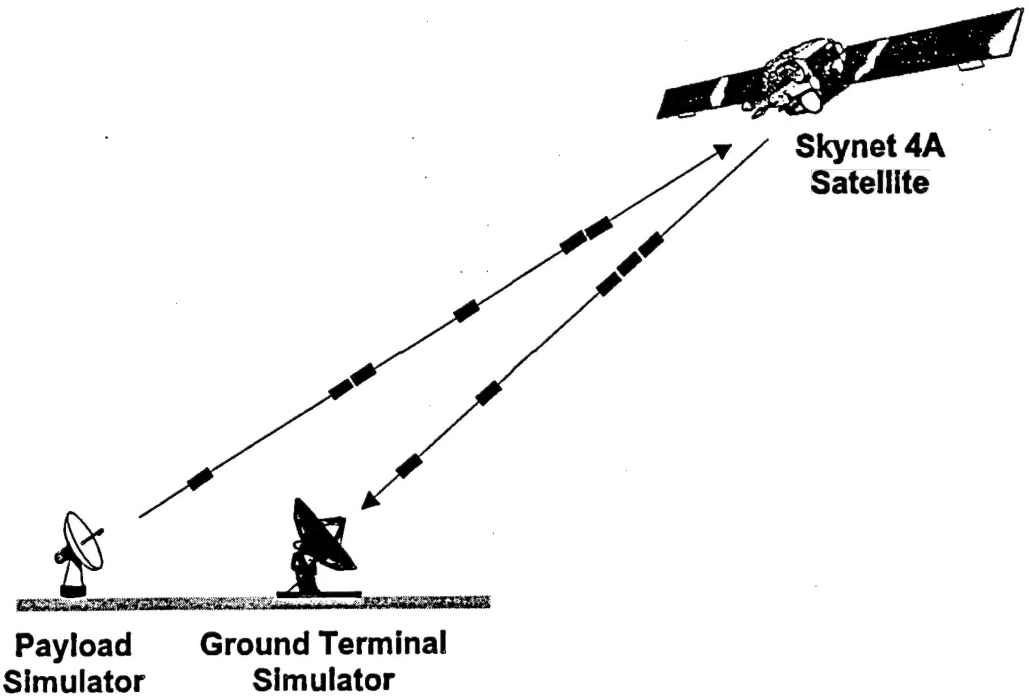


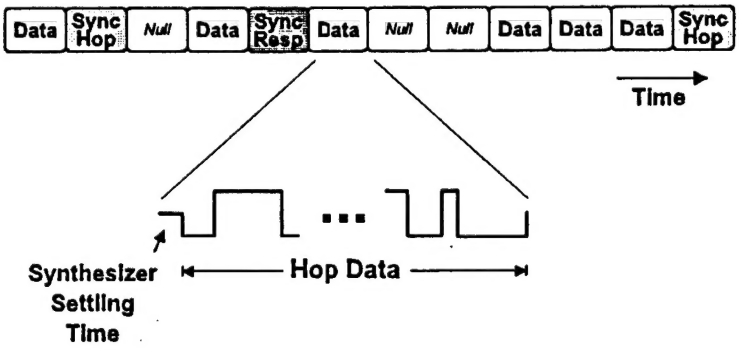
Fig. 1. EHF frequency-hopping trials setup.

This Report describes the simulators used for the EHF frequency-hopping trials. A description of the downlink FH/DPSK waveform is provided in Section 2. The transmitter portion of the payload simulator is described in Section 3. The receiver portion of the ground terminal simulator is described in Section 4. Finally, the conclusion can be found in Section 5.

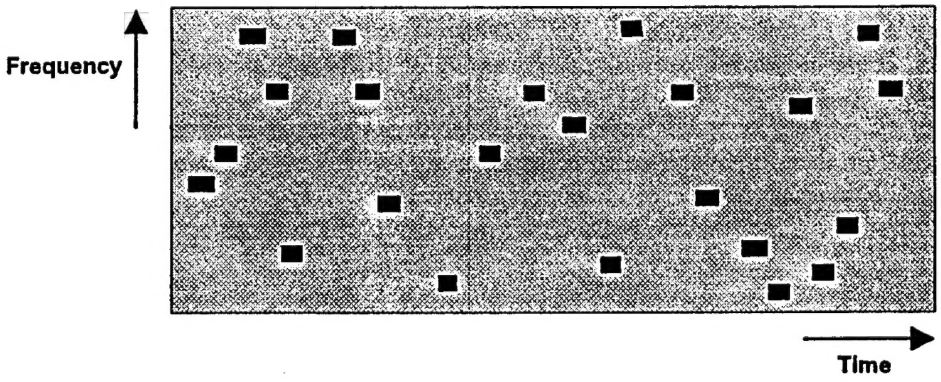
2 - Waveform Overview

The downlink waveform is based on the specification provided in [17]. As noted in the previous section however, there are some differences due to the use of Skynet 4A satellite. The waveform structure of [17] was designed for a multi-theatre environment (e.g. 32 theatres) in which a theatre is defined as a geographical area illuminated by a single or group of spacecraft antenna beams.

The payload simulator transmits four types of hops, as shown in Fig. 2(a): synchronization (sync) hops, sync response hops, data hops and null hops. A communications map is used to determine what type of hop is to be transmitted at what time and to what theatre. A collection of hops form a frame and a number of frames form a multi-frame. The communications map structure is repeated on a multi-frame basis.



(a)



(b)

Fig. 2. Frequency-hopped waveform,
(a) typical hop waveform,
(b) representative time-versus-frequency hop pattern.

The timing reference in this system is the payload simulator. This implies that the ground terminal simulator is required to adjust its timing to match that of the payload simulator. Sync hops are always included in the communications map to enable the ground terminal to achieve downlink synchronization with the payload. Sync response hops and data hops are transmitted only when a link is in the process of being established (sync response hops) or has been established (data hops). Sync response hops provide the ground terminal with timing error information to aid uplink synchronization. Data hops are formed by applying forward error correction (FEC) to the input data, packetizing the FEC output data, differentially-encoding these packets, applying packet (i.e. hop) diversity and then frequency-hopping the packets. (It should be noted that the recently completed EHF trials did not include the use of FEC.) A null hop refers to a hop duration in which nothing is transmitted by the payload simulator. The downlink waveform uses "slow hopping" in that both sync hops and data hops include multiple symbols per hop.

Fig. 2(a) also shows the hop structure. A settling time is provided at the start of each hop to allow the agile synthesizer to settle in amplitude, phase and frequency. The hop data follows the settling time to the end of the hop. A time versus frequency plot for a typical payload transmission is shown in Fig. 2(b). In this figure, the height of each hop (black rectangle) corresponds to the instantaneous bandwidth (or dehopped bandwidth) and the width corresponds to the hop duration.

Of particular interest for the EHF frequency-hopping trials over Skynet 4A is the downlink sync hop structure. The ground terminal simulator uses only sync hops to achieve synchronization in space, time and frequency with the payload simulator. The sync hops are transmitted in a burst fashion with a burst rate of approximately 3 per second. The burst format is comprised of four sync hops with a null hop between sync hops, with successive bursts separated by over 5000 hops. As a result, the communications capacity consumed (per theatre) for downlink synchronization is less than 0.1% of the total downlink capacity. A single type of sync hop is provided in [17] and is given by a 13-bit Barker code 1111100110101 with the rightmost bit representing the first bit transmitted.

In addition to the communications and synchronization signals, there were two other signals used during the experiment: the satellite beacon and the edge-of-band reference signal. The beacon is an unhopped binary phase-shift-keying (BPSK) modulated signal originating from Skynet 4A and can be found out of the communications band. Examination of the beacon power level aided in determination of spatial tracking accuracy. The edge-of-band reference signal is a low-level unhopped continuous wave (CW) signal originating from the payload simulator that was used to ensure that the transmitter was functional and to determine uplink pointing accuracy. This signal was found at the edge of the communications band but outside of the hopping band.

3 - Payload Simulator

A block diagram of the transmitter portion of the payload simulator is provided in Fig. 3. The major transmitter components and interfaces are identified in Fig. 3 and described in the subsections that follow.

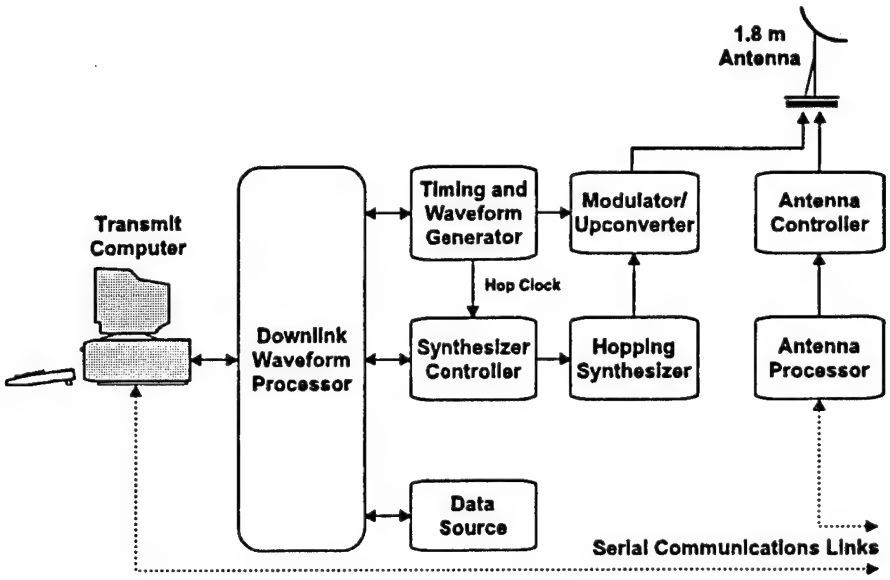


Fig. 3. Block diagram of payload simulator transmitter.

3.1 Transmit Computer

The purpose of the transmit computer is threefold: to allow local control/monitoring of the transmit waveform via keyboard input/monitor display; to enable remote control and monitoring by the Receive Computer of the transmit waveform; and to provide communications with the Downlink Waveform Processor.

The transmit computer's power-up sequence includes the execution of a transmit waveform control routine. This routine first establishes a serial communications link [18] with the Receive Computer in the Ground Terminal Simulator. The serial communications link allows the ground terminal simulator to remotely select a variety of waveforms and to observe the transmit computer status.

The routine continuously checks for local (keyboard) or remote (serial communications link) configuration commands. When a valid configuration command is received by the transmit waveform control routine, the appropriate executable code is downloaded to the Downlink Waveform Processor. After the code has been successfully downloaded, a message confirming the selected waveform is sent to the local monitor and to the Receive Computer. The routine then continues checking for additional local or remote configuration commands.

A variety of CW and frequency-hopped waveforms are available for transmission. The CW waveforms are provided primarily as an aid in link calibration. The frequency-hopped waveform options

include the transmission of sync hops only, of sync hops and fixed data, and of sync hops and user data. Data rates ranging from 2.4 kb/s to over 200 kb/s may be selected. In addition, a diversity level of 7 may be selected for the 2.4 kb/s data rate. Diversity is provided in the form of hop diversity, meaning that the hop word is repeated on multiple hops.

3.2 Downlink Waveform Processor

The Downlink Waveform Processor is a digital signal processing (DSP) board that provides the overall control of the transmit waveform. The processor tracks the time-of-day, generates the differentially-encoded hop words and ensures that they are synchronized with the correct hop frequency. The Downlink Waveform Processor is realized with a TMS320C25 processor board ('C25) developed by Spectrum Signal Processing Inc. The processor is housed within the Transmit Computer and exchanges data with the transmit computer, the Timing and Waveform Generator, the Synthesizer Controller, and the Data Source.

After the Transmit Computer receives a valid configuration command, the executable code for the selected waveform is downloaded to the 'C25. The Transmit Computer checks for a successful download and then initializes the 'C25 code, effectively starting the transmission of the selected waveform. This is the only exchange between the Transmit Computer and the Downlink Waveform Processor.

The Downlink Waveform Processor provides the Timing and Waveform Generator with time-of-day and hop word information on a hop-by-hop basis, as shown in Fig. 4. (Because there is a one-to-one correlation between the time-of-day and the hop number, the two are used interchangeably.) Fig. 4(a) shows the information flow and relative timing between the Downlink Waveform Processor and the Timing and Waveform Generator. The "Transmit Off" period was earlier introduced in Fig. 2 as the synthesizer settling time. During this period, the hop word for the current hop is provided to the Timing and Waveform Generator. The hop word contains 13 bits of differentially-encoded hop data, a Hop Enable bit and a Data/Sync bit, as shown in Fig. 4(b). The purpose of the Hop Enable bit is to limit the Timing and Waveform Generator output for null hops. The Data/Sync bit provides hop status information and is provided as a debugging aid. As discussed in Section 2, the type of hop to be transmitted is determined by comparing the communications map with the time-of-day (i.e. hop number).

Fig. 4(a) also shows the low and high words of the hop time-of-day for Hop N+1 to be provided to the Timing and Waveform Generator during Hop N. The Timing and Waveform Generator provides the Downlink Waveform Processor with a hop clock in the form of an interrupt.

Communications between the Synthesizer Controller and the Downlink Waveform Processor occur following the selection of a transmit waveform. The Downlink Waveform Processor initializes the Synthesizer Controller with the starting time-of-day, the hopping bandwidth and the base frequency (i.e. the lowest frequency within the hopping bandwidth). The Downlink Waveform Processor then enables the Synthesizer Controller to be clocked by the Timing and Waveform Generator.

Communications are provided with the Data Source for those waveform selections that include the transmission of user data. The Data Source provides a 12-bit data buffer and a status register for the Downlink Waveform Processor. When the data buffer becomes full the data full flag is set in the status register. The Downlink Waveform Processor then collects the buffered 12-bit data word for subsequent

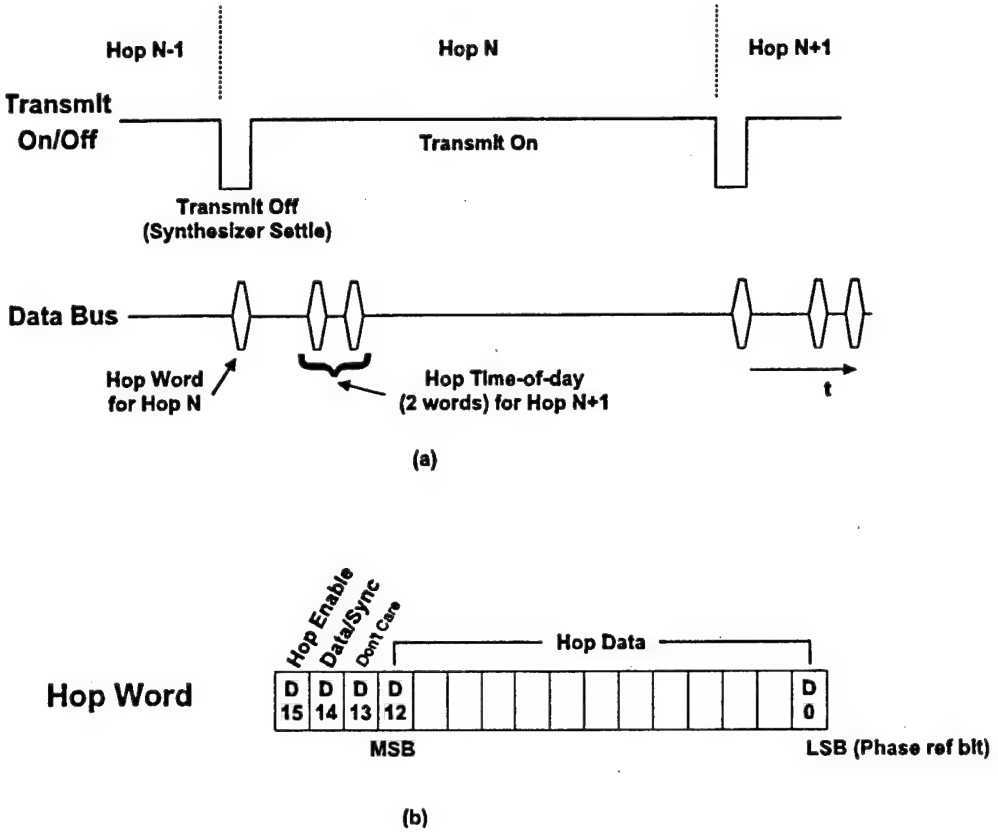


Fig. 4. Downlink Waveform Processor to Timing & Waveform Generator data exchange,
(a) time sequence,
(b) hop word composition.

differential encoding.

The Downlink Waveform Processor performs the following functions on a per hop basis:

(i) writes the hop word for the current hop (N) to the Timing and Waveform Generator within the hop settling period;

(ii) reads data from the Data Source as determined by its status register (for transmit waveforms which include user data);

(iii) prepares a hop word for the next hop (N+1) interval;

(iv) writes time-of-day for the next hop (N+1) to Timing and Waveform Generator; and

(v) increments time-of-day, frame and multiframe counters.

3.3 Timing and Waveform Generator

The Timing and Waveform Generator consists of a printed circuit board (PCB) which was developed in-house to provide the payload simulator transmitter timing signals and to generate the baseband hop waveform. A schematic of this generator is given in Appendix A. Synchronous bit, hop, analog on/off, and time-of-day data control signals are derived from an on-board crystal clock oscillator. The control signals are generated by an erasable programmable read-only-memory (EPROM) whose contents are also included in Appendix A.

The baseband hop waveform is generated by converting the hop data to an analog signal. The board also provides a 32-bit register to display the current hop number. This feature is used primarily as a debug aid. The Timing and Waveform Generator interfaces with the Downlink Waveform Processor, the Synthesizer Controller and the Modulator/Upconverter.

The Timing and Waveform Generator receives hop data, time-of-day, and analog control data from the Downlink Waveform Processor and provides it with a hop clock. The Timing and Waveform Generator also provides the Synthesizer Controller with the same hop clock signal. This ensures that the time-of-day counter on-board the Downlink Waveform Processor is synchronized to the hop frequency generated in the Synthesizer Controller.

The Timing and Waveform Generator also provides a baseband analog signal that is applied to the Modulator/Upconverter.

3.4 Synthesizer Controller

The Synthesizer Controller consists of a Hopping Controller Interface and a Hopping Synthesizer Controller. Synthesizer Controller interfaces with the Downlink Waveform Processor, the Timing and Waveform Generator and the Hopping Synthesizer.

The Hopping Controller Interface reformats the data received from the Downlink Waveform Processor for the Hopping Synthesizer Controller. The hop clock received from the Timing and Waveform Generator and the reformatted data are applied to the Hopping Synthesizer Controller. A schematic of the Hopping Controller Interface is included in Appendix B.

The Hopping Synthesizer Controller receives initialization data (hopping bandwidth, base frequency and time-of-day) from the Downlink Waveform Processor. In addition, the controller implements a 31-bit multiplicative linear congruential random number generator from which the nominal hop frequency is derived. A detailed description of the Hopping Synthesizer Controller is provided in [12].

3.5 Data Source

The Data Source consists of a Data Source Interface Board and one of two plug-in data sources. The schematic for the Data Source Interface Board is provided in Appendix C. This board includes a status register to provide an indication of data availability, and a 12-bit data register that may be read by

the Downlink Waveform Processor. The Data Source Interface Board may be connected to either an HP 1654A Bit-error-rate Test Set or an linear-predictive-coder (LPC) via an RS-232 link, and is currently configured to provide data at a rate of 2.4 kb/s.

3.6 Hopping Synthesizer

The Hopping Synthesizer is realized using a Comstron FS2000 Frequency Synthesizer. The unit is commanded, by the Synthesizer Controller through a 44-bit parallel binary-coded-decimal (BCD) port, over a range of 646 - 696 MHz with a frequency resolution of 100 Hz. The Hopping Synthesizer settling time is specified at less than 1 μs. The output of the Hopping Synthesizer is applied to the Modulator/Upconverter.

3.7 Modulator/Upconverter

A system diagram of the Modulator/Upconverter is provided in Appendix D. The frequency-hopped carrier supplied by the Hopping Synthesizer is mixed with the analog baseband hop waveform supplied by the Timing and Waveform Generator. The nominal 700 MHz output signal from the mixer is filtered and applied to an in-house developed 44/20 GHz Transceiver [19]. The diagram for the 44/20 GHz Transceiver is also provided in Appendix D. The output of the transceiver is applied to a 40 watt travelling-wave-tube amplifier (TWTA) and subsequently to the antenna feed.

3.8 Antenna, Ephemeris Processor and Antenna Controller

The transmit antenna system used for the Skynet EHF trials is a fully steerable, pedestal mounted 1.8 m parabolic dish. It is located in a radome on top of Building 2 at the CRC. The Antenna Controller for this pedestal was developed by Scientific Atlantic and has a pointing accuracy of +/- 0.003 degrees. For the EHF trials, the updated azimuth and elevation pointing information was provided to the controller every 10 seconds by the Ephemeris Processor. It should be noted that Skynet 4A is geosynchronous but not stationary hence required continuous tracking during the experiment.

The Ephemeris Processor has the ability to provide independent control of the antenna by using tracking data from the "Orbital Workbench" orbital prediction package from Cygnus Engineering. The Ephemeris Processor also has a serial communications link with the ground terminal simulator's Ephemeris Processor (which has its own ephemeris prediction package) and can be controlled remotely if required. See Section 4.8 for more details on this remote control.

4 - Ground Terminal Simulator

A block diagram of the receiver portion of the ground terminal simulator is provided in Fig. 5. The major receiver components and interfaces are identified in Fig. 5 and described in the subsections that follow. Since the Data Logger has serial communications links with all of the computers, the individual links are not shown in Fig. 5.

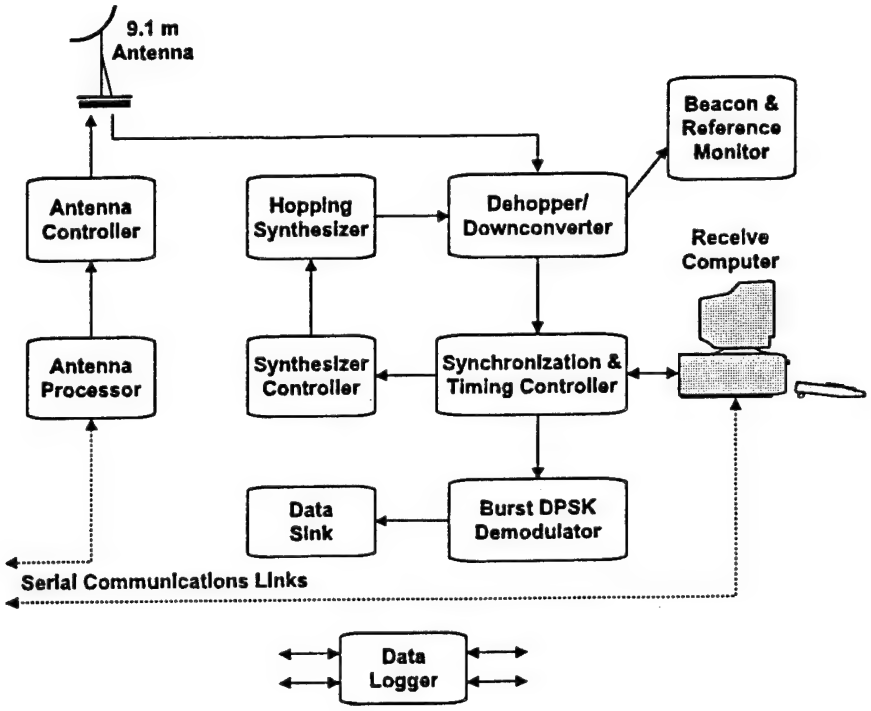


Fig. 5. Block diagram of ground terminal simulator.

4.1 Receive Computer

The Receive Computer provides local control over the ground terminal's synchronization process as well as remote control of the payload simulator's transmit waveform through a serial communications link. After the operator has invoked the synchronization routine, the Receive Computer communicates with the Synchronization and Timing Controller and provides limited processing of the dehopped signal, real-time monitoring of the ground terminal's synchronization performance and logging of a variety of synchronization estimation parameters both locally and to a Data Logger via the serial communications link.

The synchronization routine first establishes a serial communications link with the Receive Computer and the Data Logger. The routine then initializes the DSP and analog-to-digital (A/D) boards included in the Synchronization and Timing Controller. A detailed description of the hand-shaking

procedure between the Receive Computer and the Synchronization and Timing Controller is provided in Appendix F.

4.2 Synchronization and Timing Controller

As shown in Fig. 6, the Synchronization and Timing Controller has interfaces with the Dehopper/Downconverter, Burst DPSK Demodulator and Synthesizer Controller. The Synchronization and Timing Controller includes an IF chain (Fig. 7) which provides for injection of test signals and noise, for monitoring the dehopped waveform, and for envelope and quadrature detection. It also includes two in-house developed circuit boards (the Analog Baseband Board and the Timing and Control Board) and two commercial off-the-shelf boards (a Spectrum TMS320C25 DSP board and a Metrabyte DAS 50 A/D board). The Spectrum board features a DSPLINK interface, as documented in [20], which provides high speed parallel connection from the DSP to peripherals.

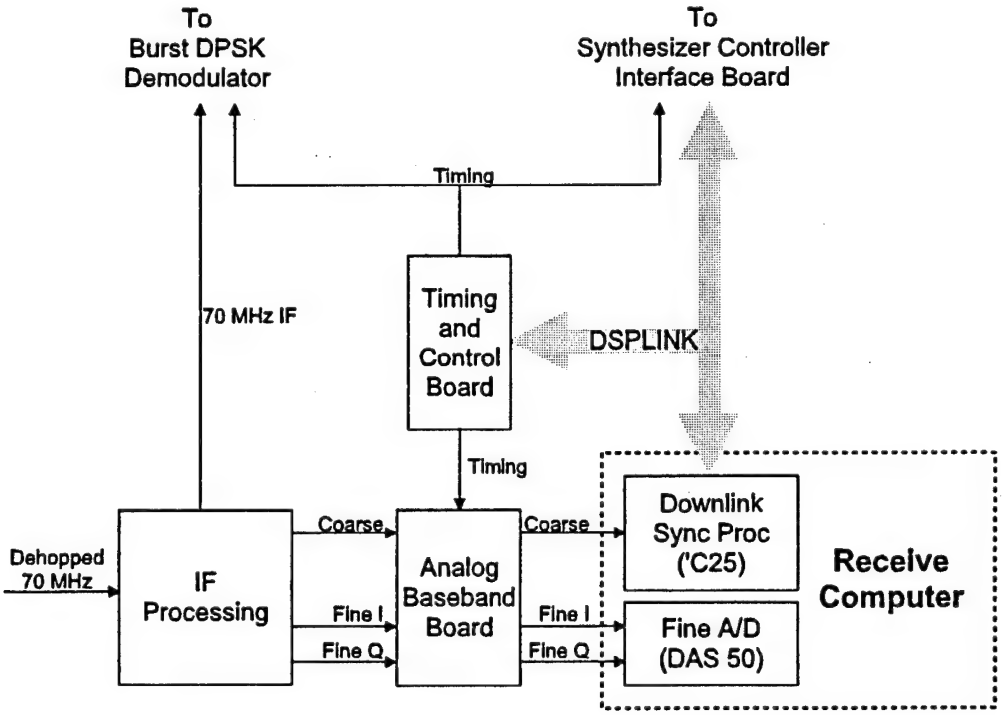


Fig. 6. Synchronization and Timing Control block diagram.

The Dehopper/Downconverter provides the Synchronization and Timing Controller with a dehopped waveform at a nominal frequency of 70 MHz. This signal is attenuated, summed with a user injection port signal, bandpass filtered and then split into three paths. One path is provided to the Burst Demodulator, the second is used for the envelope detection and the third is used for quadrature detection. The envelope detected signal and quadrature baseband signals are then provided to the Analog Baseband Board, which is described in detail in Appendix E. In summary, the Analog Baseband Board applies integrate-and-dump and sample-and-hold techniques to the input waveforms using the control signals

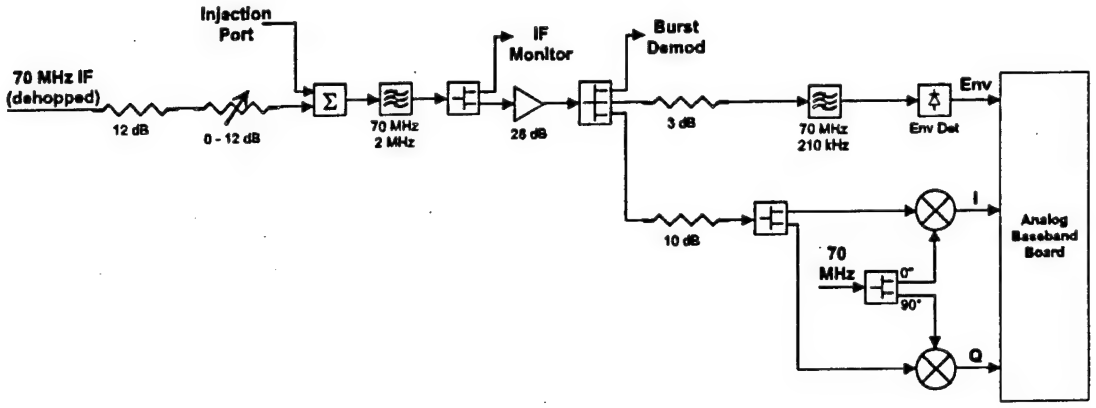


Fig. 7. IF processing for Synchronization & Timing Control.

provided by the Timing and Control Board. The envelope detection output from the Analog Baseband Board is applied to the Downlink Synchronization Processor which is a commercial DSP board hosted by the Receive Computer. The quadrature-detected signals are applied to a DAS 50 A/D board which is also hosted by the Receive Computer.

4.2.1 Hosted Off-the-shelf Boards

A Spectrum Signal Processing 'C25 DSP processing board was selected to realize the Downlink Synchronization Processor functional requirements. The Downlink Synchronization Processor modifies the reference hop clock phase and rate by writing, through DSPLINK parallel interface on the Timing and Control Board, to a numerically controlled oscillator (NCO) phase-accumulator register. The Downlink Synchronization Processor supplies the Timing and Control Board with the current hop time of day, also via the DSPLINK interface. The board includes a single channel relatively slow A/D converter to process the envelope detected waveform. The processor provides the majority of the receive signal processing functions such as estimates of bit timing error, clock rate error and carrier frequency offset. The synchronization algorithm used to compute these values is described in Appendix F. The processor also maintains a variety of counters including the time-of-day and hop number within a frame. The counters are incremented on a hop basis, with the hop clock reference provided by an interrupt from the Timing and Control Board.

The Metrabyte DAS 50 A/D board is used for fine synchronization. It is a 4-channel, 12 bit A/D board which may be clocked at up to 1 Msample/s and stores up to 1 Mword. The DAS 50 trigger control, arming control, and channels select are set up through the PC bus by the Receive Computer. The board is armed by the PC with the sample trigger provided by the Timing and Control Board. Approximately nine hops of data are collected by the DAS 50 board, in order to digitize the entire sync hop burst plus an additional hop on either side of the burst. The stored data is then read by the Receive Computer and subsequently written to the Downlink Synchronization Processor.

4.2.2 In-house Developed Boards

The Timing and Control Board was realized with an in-house developed PCB. A schematic of the Timing and Control Board is provided in Appendix G. This board uses a 32-bit NCO to achieve a

variable reference clock. The input clock to the NCO is a 40 MHz crystal oscillator. The initial reference clock frequency is downloaded from the 'C25 as a 32-bit Δ-phase register. This Δ-phase value is added at each clock tick so there is a one-to-one correspondence with the output reference clock frequency. During verification and track mode, the 'C25 changes the Δ-phase value temporarily to adjust output clock phase or changes the value for an indefinite period to adjust the output clock rate.

The NCO output is fed to a fast D/A and filtered to generate a sinusoidal reference. This is then input to a fast comparator to generate a digital reference clock. The digital reference clock is divided down before clocking a timing generator EPROM which supplies receiver boards with control signals (such as hop clock, bit timing signal, envelope-detection and quadrature-detection timing signals). A 32-bit hop number (which corresponds to the time-of-day) is provided for debug purposes.

Downlink synchronization processing is done primarily on a hop basis, so the hop clock from the Timing and Control Board is used to interrupt the 'C25. Clocking and data hop control signals are provided to the Burst DPSK Demodulator. Sample/hold, integrate/dump signals are provided to the Analog Baseband Board. The Timing and Control Board also provides the 'C25 with the data capture status of the DAS 50 A/D board hosted in the PC. Synthesizer frequencies are changed at the beginning of each hop, so the hop clock is supplied to the Synthesizer Controller Interface Board to be passed to the Hopping Synthesizer.

Fig. E1 provides a schematic of the Analog Baseband Board. The board includes a single channel for the envelope detected signal and two channels for the in-phase and quadrature-phase detected signals. Two paths for each channel are used in a ping-pong fashion to eliminate losses that would otherwise result in a single path that would have to allow for dump time. The envelope and quadrature detected signals are amplified, filtered, and then applied to integrate-and-dump and sample-and-hold circuits. Transistor-transistor-logic (TTL) timing signals provided by the Timing and Control Board are converted to a bipolar levels by the Analog Baseband Board to control the many analog switches.

4.3 Synthesizer Controller

The Synthesizer Controller was earlier described in Section 3.4 for the payload simulator. The ground terminal simulator Synthesizer Controller also consists of a Hopping Controller Interface and a Hopping Synthesizer Controller. The Hopping Synthesizer Controller interfaces with the Synchronization and Timing Controller and the Hopping Synthesizer.

The only difference between the ground terminal simulator Synthesizer Controller and the payload simulator Synthesizer Controller is the use of a special synchronization mode which allows the Hopping Synthesizer to be rapidly transitioned from one predetermined sync hop frequency to another. This capability is exploited only during synchronization acquisition mode. More details of this mode can be found in Appendix F.

4.4 Hopping Synthesizer

The Hopping Synthesizer used with the ground terminal simulator is the same as described for the payload simulator in Section 3.6.

4.5 Dehopper/Downconverter

A diagram of the Dehopper/Downconverter is provided as Appendix H. The signal from the payload simulator is received via Skynet 4A at the 9.1 m antenna, located at DREO, and fed through a Miteq low-noise amplifier (LNA). This signal is then split into two paths: communications (including sync hops, data hops and edge-of-band reference signal) and beacon.

The signal in the beacon path is filtered and then downconverted to 10.7 MHz to isolate the Skynet 4A beacon. This signal is split to provide beacon and beacon squared (since the beacon is BPSK modulated, squaring removes all modulation). The beacon squared is derived by limiting, amplifying and finally multiplying the beacon by itself. The beacon (10.7 MHz) and beacon squared (21.4 MHz) are two of the three signals summed for the Beacon and Reference Monitor. The Beacon and Reference Monitor was used to monitor the power and noise levels during the experiment.

The signal in the communications path is amplified and then split into the sync/data signal and the edge-of-band reference signal. The reference signal (an unmodulated carrier) is downconverted to 70 MHz, filtered and then becomes the third of three signals summed for the Beacon and Reference Monitor. The sync/data signal is dehopped and downconverted to a nominal 70 MHz. This is then split into four paths (only three are shown on the diagram): Comstream modem, coarse synchronization, fine synchronization and data. The Comstream modem path is used during channel characterization and is not used while hopping. The coarse synchronization path includes an envelope detector. The fine synchronization path and data path are identical in that they include a quadrature downconversion to baseband. The in-phase (I) & quadrature-phase (Q) outputs for fine synchronization go to the DAS 50 A/D board hosted in the PC whereas the I & Q outputs for data go to the Burst DPSK Demodulator (not shown in Appendix H).

4.6 Burst DPSK Demodulator

The Burst DPSK Demodulator consists of a PC hosting a TMS320C25 DSP and two external in-house boards: the Burst DPSK Demodulator Analog Board and the Data Sink and A/D Interface Board. The analog board takes the I & Q baseband signals from the Dehopper/Downconverter, integrates them over a bit period, sample/holds them and finally A/D converts them, providing digital values for I & Q. The timing signals for the analog board come from the Data Sink and A/D Interface Board.

The Data Sink and A/D Interface Board buffers both I & Q input samples in a common first-in-first-out (FIFO) memory to be read by the DSP. Once the I & Q data is received in the DSP, demodulation is done. For DPSK, the dot product of the previous complex (I & Q as a vector) sample with the current complex sample provides a value who's sign indicates whether the phase differs by 180° (-) or 0° (+). This sign is used to decide on a differentially encoded '1' or '0'. Note that there is a fixed reference bit prior to the first data bit. If time diversity is being used, the demodulator also does majority logic combining over several hops (in these trials diversities of 1 or 7 were used). Once the hops are combined, the data is then output to the Data Sink described in the next section.

The Data Sink and A/D Interface Board also provides the data clock and received data from the DSP to be sent serially to the data sink device. The Data Sink and A/D Interface Board has one shift register and one holding register for data going to the Data Sink. The schematics for the Burst DPSK Demodulator Analog Board, and the Data Sink and A/D Interface Board can be found in Appendix I.

4.7 Data Sink

The Data Sink for these trials consisted of either an HP 1654A Bit-error-rate Test Set for performance measurements or a 2.4 kb/s linear-predictive-coder (LPC) for digital voice tests. One or the other was connected through the Data Sink and A/D Interface Board described in the previous section.

4.8 Antenna, Ephemeris Processor and Antenna Controller

The receive antenna system used a fully steerable, pedestal mounted 9.1 m dish having a 0.3° 3 dB-sidelobe. It is located in an outbuilding at DREO. The receive antenna is controlled by an Andrew/Kintec controller.

The Ephemeris Processor consists of a PC-compatible at the receive site (DREO) that points the receive antenna and provides pointing information to the transmit site. At the transmit site, another PC-compatible takes this information and drives the Scientific Atlanta controller to steer the transmit antenna. The orbital prediction for the satellite is done offline using the Orbital Workbench software package from Cygnus Engineering to provide high precision propagation of state vector elements and pointing vectors. The pointing data predictions for at least a week are then transferred to the Ephemeris Processor to interpolate these and supply real-time pointing to the antenna systems.

4.9 Beacon and Reference Monitor

The Beacon and Reference Monitor measures the signal power, noise power and frequency of three signals: beacon, beacon squared and edge-of-band reference. These signals are obtained from the Dehopper/Downconverter. These values are logged continuously as part of the experiment to ensure any problems (due to weather or equipment failure) that occur during synchronization or data communications can be isolated to the relevant equipment. For example, if the beacon is still good, but the edge-of-band reference signal disappears, one should suspect the transmitter. If the signal-to-noise ratio on the edge-of-band reference signal decreases (but not that of the beacon), one should suspect rain or heavy clouds. The frequency measurements are used to determine frequency offsets of the equipment and the Skynet 4A transponder.

4.10 Data Logger

The Data Logger consists of a PC-compatible running an in-house real-time data storing package which is detailed in [21]. The program was written in Microsoft 'C' V7.0 and uses the serial communications links to all the other computers. The Data Logger is connected to a GOES time distribution satellite clock and distributes accurate time-of-day information to all computers. Any messages received by the logger are stored in a file along with periodic logging of the time. The software is designed to be as robust as possible by not using the normal 'C' and DOS buffers. This results in minimal logging losses in the event of power interruptions.

5 - Conclusion

The Skynet EHF Downlink Trials were successfully run in week-long experiments over two years. Frequency-hopped spatial and time synchronization were achieved. Data and voice communications were demonstrated with and without time diversity. Problems with the commercial frequency hopping synthesizers precluded the completion of some of the data communications experiments in the time available.

These trials provided the MILSATCOM groups an opportunity to research robust satellite frequency-hopped synchronization and communications. This experience has proven invaluable in the support of the D6470 project, specifically for the EHF system simulator being developed in industry.

Work has already begun for Skynet EHF Uplink Trials to work on the other aspect of system synchronization as well as examining frequency-shift-keying (FSK) modulation for uplink data. Once this work at low-data-rates (LDR) is complete, consideration should be given to future trials at medium data rates (MDR) since the demand for data in the modern military environment is continuously increasing.

6 - References

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20. *TMS320C25 Processor Board User's Manual Version 2*, Spectrum Signal Processing Inc., Burnaby, Canada, September 1988.

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Appendix A

Timing and Waveform Generator Board

This appendix provides the details of the Timing and Waveform Generator Board. Fig. A1 is the Timing and Waveform Generator Board schematic. Fig. A2 shows the waveform output of the Transmit Control Signals EPROM.

The Timing and Waveform Generator Board is connected to the Transmit Processor 'C25 via the DSPLINK interface. The DSPLINK address assignments and bit fields are detailed below.

Address	Read/Write	Register
10	Write	Hop Number Low Word (16 bits)
11	Write	Hop Number High Word (16 bits)
12	Write	NCO Control D0 NWr: 0 to write 8-bit data D1 LdStb: 1 to load new Δ-phase (after all 32 bits loaded) D2-D15 *not used*
13	Write	NCO Address/Data D0-D7 NCO Data (8 bits) D8-D9 NCO Address (2 bits) 00 for LSB, up to 11 for MSB D10-D15 *not used*
14	Write	Board Control D0 Data Hop: 1 during data hop D1 Clear A/D Done: 1 to clear A/D Done Latch D2-D15 *not used*
15	Read	Board Status D0 A/D Done Latch: 1 for A/D conversion complete D1-D15 *not used*

Fig. A2 shows the waveform output of the Transmit Control Signals EPROM. Eight bits (D0 to D7) are output at each clock tick. The diagram has vertical lines at every four bytes. In general, the data value is constant over four addresses, but in two cases it changes within the four bytes (addresses 0-3 and 104-107). Note as well that the EPROM address counter is reset after address 107 so that addresses 108 and higher are never used.

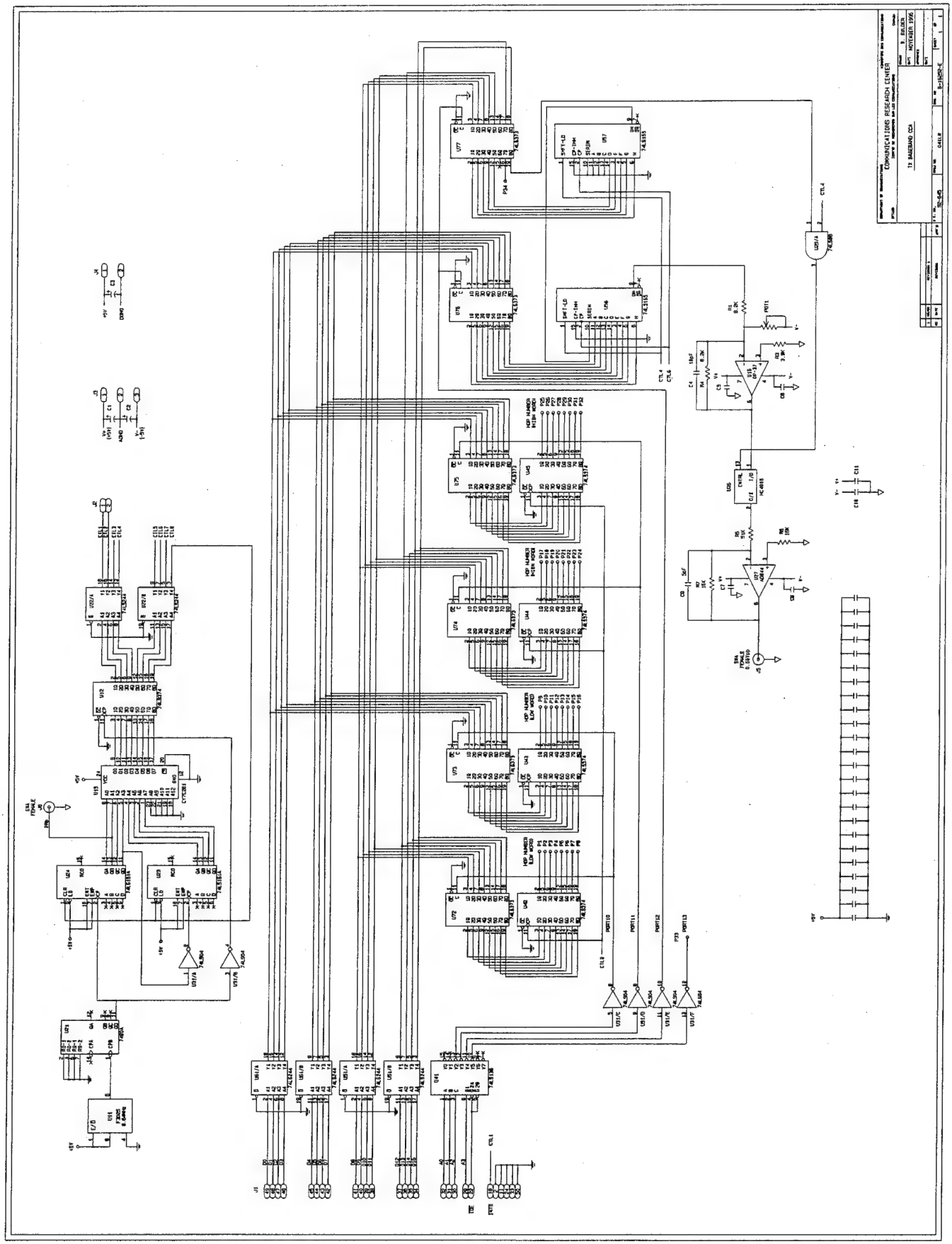


Fig. A1. Timing and Waveform Generator Board schematic.

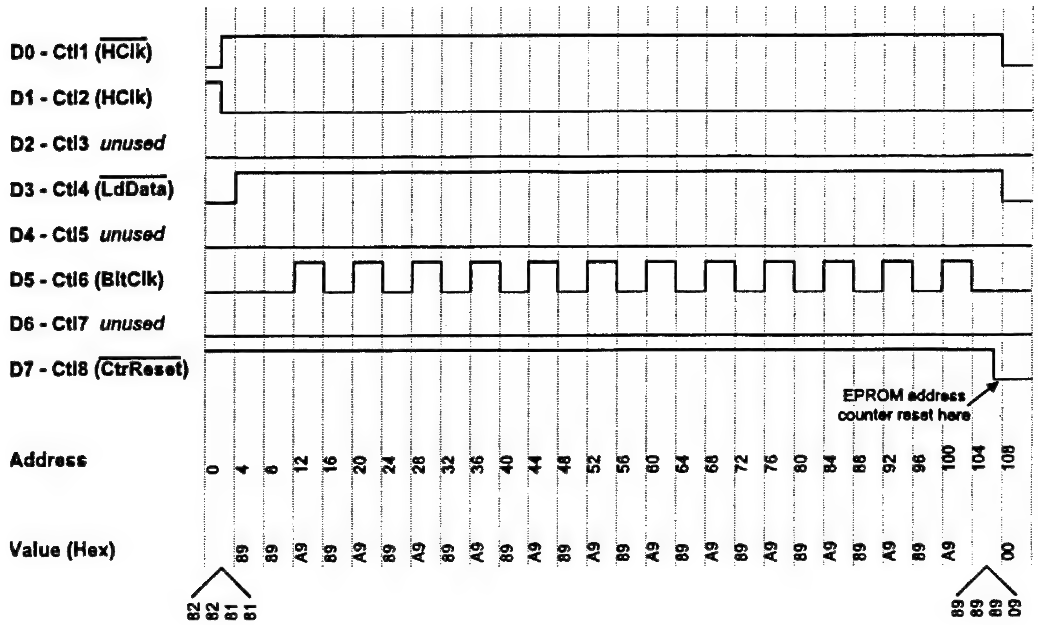


Fig. A2. Transmit Control Signals EPROM.

Appendix B

Hopping Controller Interface Board

This appendix provides the details of the Hopping Controller Interface Board. The schematic can be found in Fig. B1. This board is connected to the Transmit Processor or the Downlink Synchronization Processor 'C25 via the DSPLINK interface. The DSPLINK address assignments and bit fields are detailed below. More details on the Hopping Synthesizer Controller can be found in [12].

Address	**Read/Write**	**Register**
5	Write	Data (16 bits)
6	Write	Control D0-D14 *not used* D15 Strobe: rising edge causes controller to latch data
7	Read	Status D0 Sync: 1 = ready to proceed in special sync mode (all computations done) D1 Ready: 1 = ready to receive more data D2-D15 *not used*

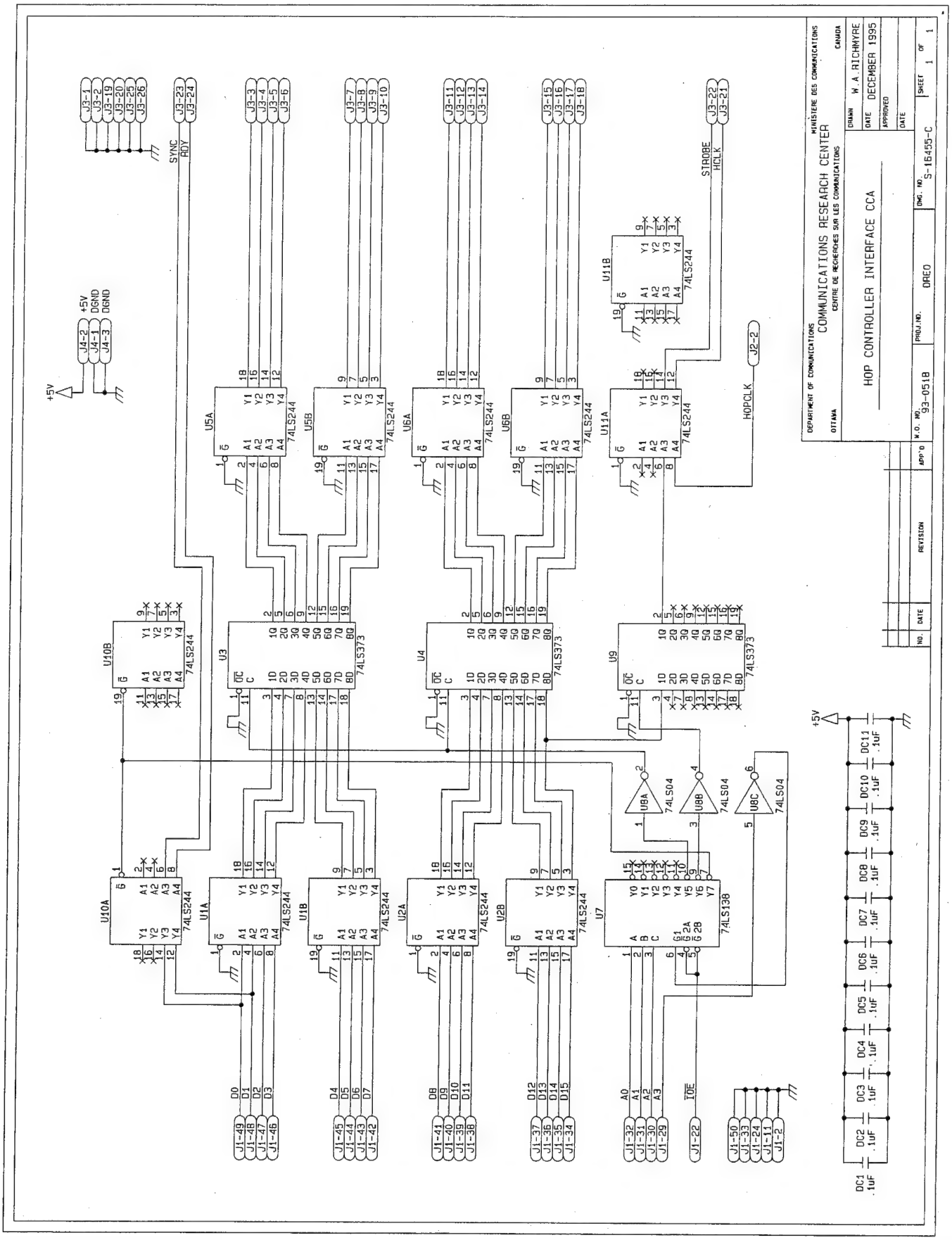


Fig. B1. Hopping Controller Interface Board schematic.

Appendix C

Data Source Interface Board

This appendix provides the details of the Data Source Interface Board. The schematic can be found in Fig. C1. This board is used to interface to a 2.4 kb/s LPC or a HP 1645A Bit-error-rate test set. The board also connects to the Transmit Processor through the DSPLINK. The address used on this board is switch selectable to 0, 2, 4, 6, 8, 10, 12, or 14. The DSPLINK registers (for a base address switch setting of 0) and bit fields are detailed below.

Address	Read/Write	Register
0	Read	Receive Data (12 bits): LSB is first bit received
0	Write	Transmit Data (12 bits): LSB is first bit sent
1	Read	Status D0 Hop Rising Edge Latch: 1 after hop clock rising edge (reset after status read) D1-D11 *not used* D12 Transmit Hold Underflow: 1 = not enough transmit data (reset by write to transmit data) D13 Transmit Hold Empty: 1 = ready for new transmit data (reset by write to transmit data) D14 Receive Data Overflow: 1 = receive data lost because the old data was not read in time (reset by read from receive data) D15 Receive Data Ready: 1 = receive data ready (reset by read from receive data)
1	Write	Command D0 Reset: 1 forces hardware reset (this value is not latched so there is no need to clear it afterwards) D1-D15 *not used*

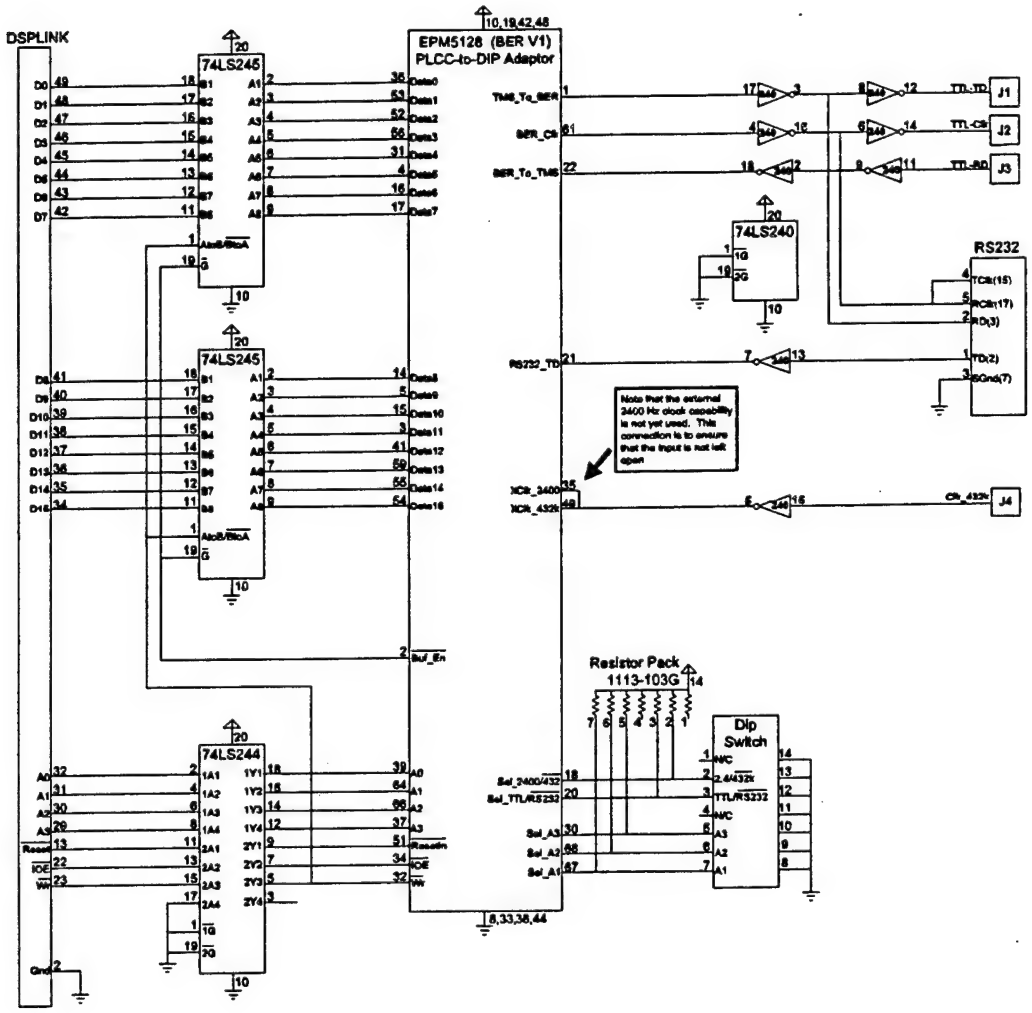


Fig. C1. Data Source Interface Board schematic.

Appendix D

Modulator/Upconverter

This appendix provides the details of the Modulator/Upconverter. The system diagram can be found in Fig. D1. Details of the 44/20 GHz Transceiver are shown in Fig. D2 and further information can be found in [19].

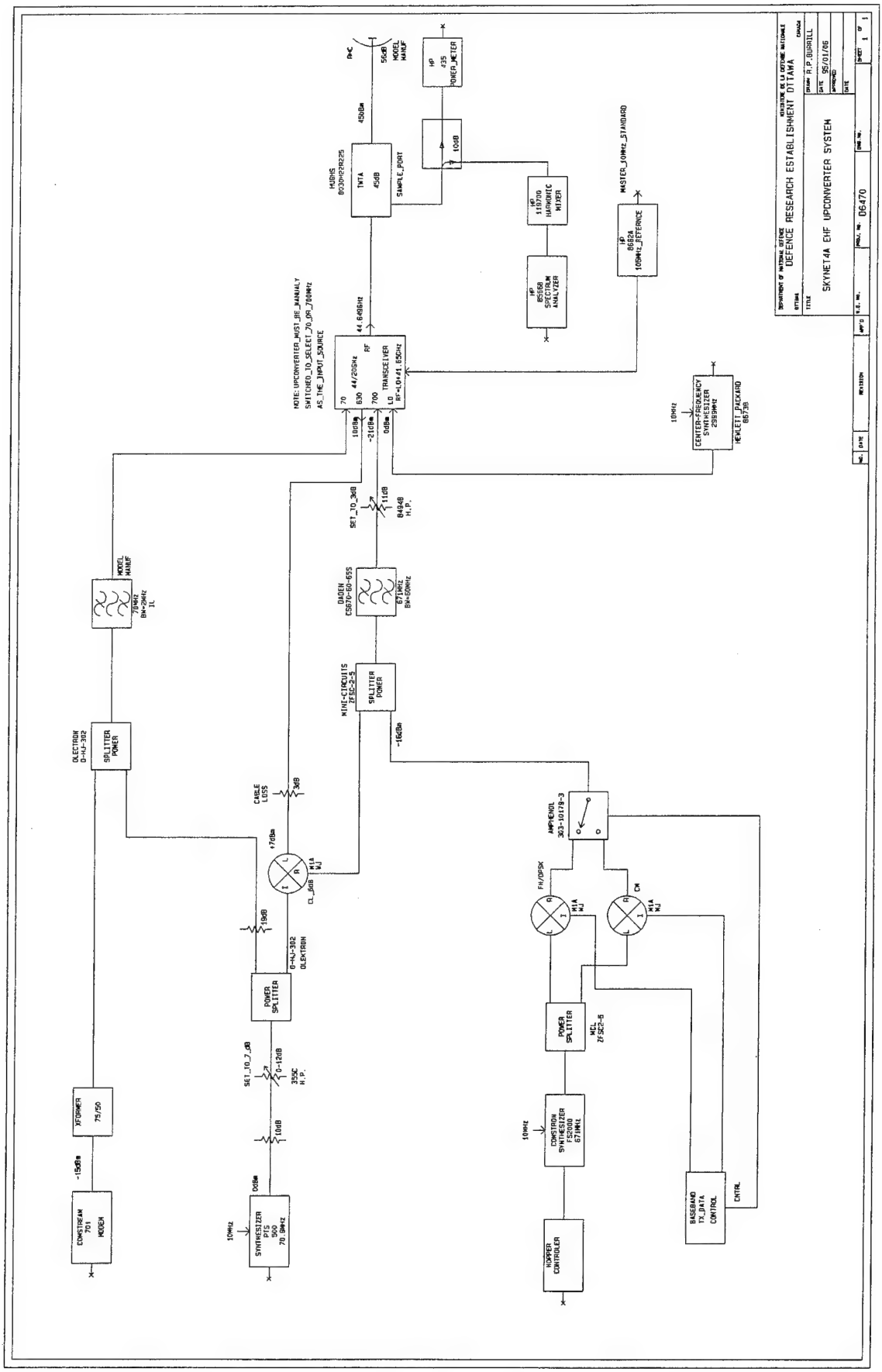


Fig. D1. Modulator/Upconverter System diagram.

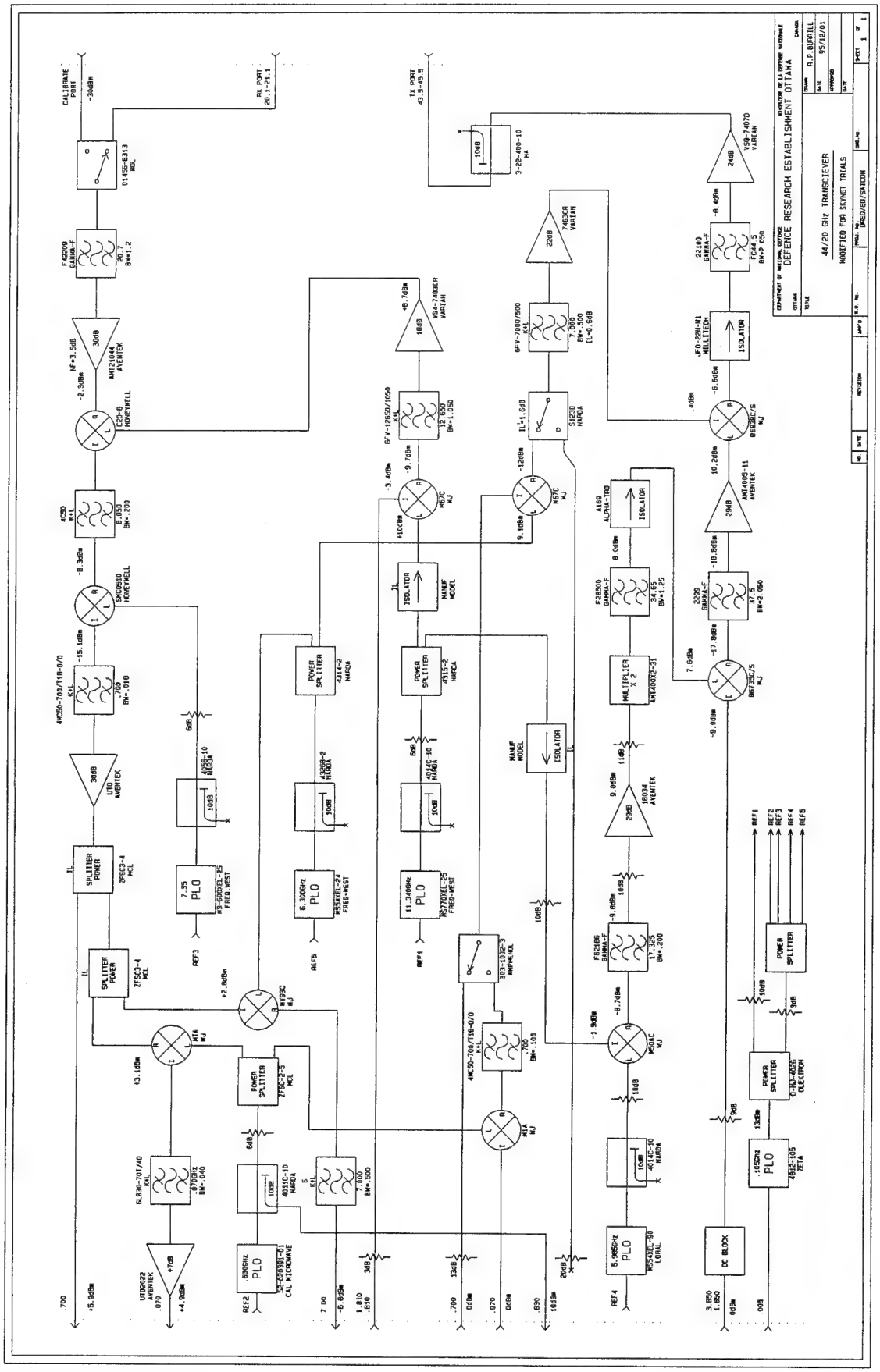


Fig. D2. 44/20 GHz Transceiver Detail diagram.

Appendix E

Analog Baseband Board

This appendix provides the details of the Analog Baseband Board used in the receiver. The schematic is shown in Fig. E1. This board is used to integrate and sample/hold the analog baseband signals. Also, the control signals are converted from TTL levels to the levels necessary to drive the analog switches.

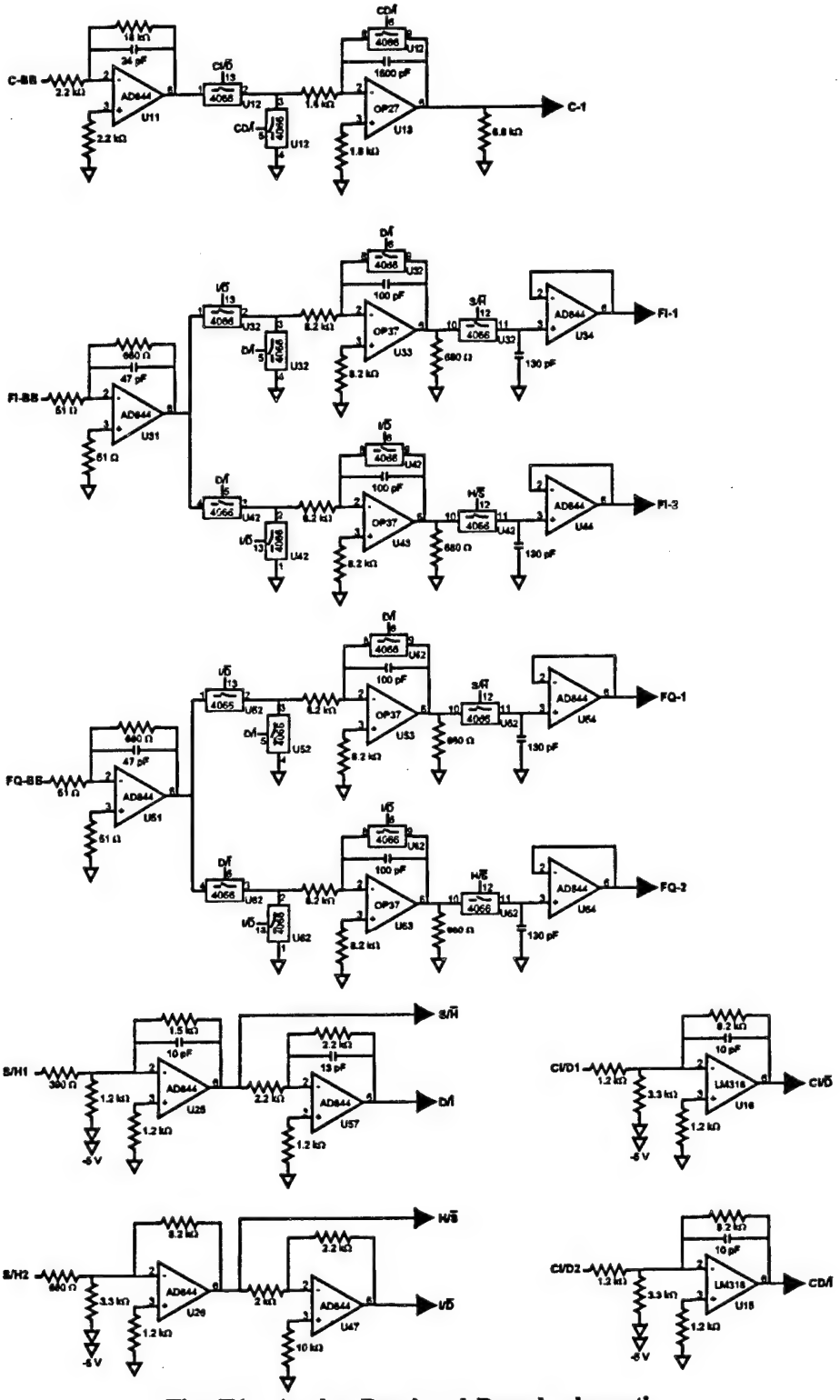


Fig. E1. Analog Baseband Board schematic.

Appendix F

Synchronization Algorithm

F-1 Introduction

The purpose of this Appendix is to describe the synchronization process, and the hardware/software implementation and interaction. As discussed in Section 4.2, all baseband synchronization activities are performed using a DSP board, an A/D board and the host computer.

The synchronization process at the ground terminal simulator can be separated into three distinct modes: acquisition, verification and tracking. The synchronization process starts in the acquisition mode and only exits this mode after the first three sync hops (from the burst of four) have been detected or by an operator keyboard input. Recall from Section 2 that sync hops are transmitted in bursts of four with successive sync hops separated by one hop period. While in acquisition mode, only the envelope of the dehopped data is processed, and it must of course be processed in real-time. The envelope-detected signal is sampled at a rate in excess of 50 kHz using an A/D converter on the DSP board. After the third sync hop has been detected, the A/D board is triggered thereby allowing both the envelope and quadrature-detected signals to be digitized. Detection of the third sync hop transitions the synchronization process to verification mode.

The verification mode begins with the last hop from the detected sync hop burst and ends after collecting two complete sync hop bursts. The purpose of the verification mode is to provide an initial estimate of the relative timing errors for bit timing offset. The estimate is achieved by using first the coarse or envelope-detected data followed by the fine or quadrature-detected data. In other words, the verification mode seeks to provide an initial correction of both the clock phase error and the clock rate error. The timing error estimate derived from the coarse data reduces the timing uncertainty to a fraction of a hop [2]. A receiver timing error estimate of a fraction of a bit [2] is obtained from this single sync hop for the range of Eb/No of interest. The receiver timing estimate is corrected prior to the next sync hop burst. This estimate allows for a relatively narrow timing uncertainty window that must be searched using the more computationally expensive quadrature-detection data. The next two sync hop bursts are collected and processed to compute the hop clock rate error and bit timing error estimates. The receiver timing reference is adjusted appropriately, and the synchronization process enters tracking mode.

The purpose of the tracking mode is to monitor, correct and log the relative errors in receiver bit timing, hop clock rate, and dehopped frequency as well as to estimate the sync hop power and noise power.

Two separate but obviously related routines were developed for the PC and the DSP for synchronization. The routine used for the PC was written in 'C' and was entitled "SYNC" while that for the DSP was in Texas Instruments's 'C25 Assembly Language and was entitled "RX". The signal processing functions associated with each routine and the communications between the PC and the DSP and A/D boards will be described for the three synchronization modes in the following sections.

F-2 Pre-synchronization Activities

A FH/DPSK transmit waveform must first be selected before starting the downlink synchronization routines. This may be achieved by entering the selection locally at the Transmit Computer console or remotely at the Receive Computer via the "CWFINE" or "SCAN" routines. Optionally, one may modify "SYNC" to allow the operator to define a waveform before beginning synchronization or by writing a simple routine whose sole purpose is to allow the operator to specify a candidate waveform.

To bring up a waveform from the Receive Computer, one may type "CWFINE". Once the routine has been loaded the user enters "m" which is short for mode. The operator is then provided with a list of waveform selections. The frequency-hopping selections include:

Key	Sync Hops	Data Source	Data Rate	Data Diversity	Frequency Hopping
"5"	on	no data	n/a	n/a	on
"6"	on	fixed word	> 200 kb/s	1	off
"7"	on	fixed word	> 200 kb/s	1	on
"8"	on	fixed word	2.4 kb/s	1	on
"9"	on	BER/LPC	2.4 kb/s	1	on
"0"	on	BER/LPC	2.4 kb/s	7	on

Assuming that all required equipment has been turned on and that the desired transmit waveform has been selected, the operator may start the synchronization process by typing "SYNC" at the Receive Computer's console. Doing so causes the PC (i.e. the 'C' routine) to first establish serial communications with the Transmit Computer, Ephemeris Processor and the Data Logger as required by the "serial.cfg" data file [18]. The 'C' routine then waits for Data Logger to provide the system date and time.

After receiving the system date and time, the 'C' routine then opens a file for data collection. The tracking loop filter parameters, discussed in more detail in Section F-4, are then initialized. The DAS 50 board, a 4-channel A/D board with 1 Mword storage, is subsequently initialized. The DAS 50 board is used to collect the quadrature-detected sync hop burst.

Throughout the initialization and synchronization procedures, the keyboard and serial communications message buffers are continually polled to allow the operator to exit the synchronization routines.

F-3 Acquisition Mode

The 'C' routine initializes the 'C25 board and downloads its executable code. The 'C' routine then starts the DAS 50 board which subsequently waits for an external interrupt. This interrupt is supplied at the end of the acquisition mode (i.e., after the first three sync hops of a burst of four have

been detected). The 'C' routine starts the 'C25 board and then waits for the DSP to write to a communications register. If a write does not occur within approximately 4 seconds, the 'C' routine "times out". A message is sent to the screen that acquisition was not achieved for this attempt, followed by a re-initialization of the 'C25 and DAS 50 boards.

The 'C25 board is kept quite busy in acquisition mode. It matched filters the envelope-detected signal (i.e. sums up the most recent 3 samples) and checks for detection using constant false-alarm rate (CFAR) processing

Separate thresholds are used for detecting the first and subsequent sync hops. This was done to keep the false alarm rate low for the first sync hop and maintain as high a probability of detection for the second and third sync hops as practical.

F-4 Verification Mode

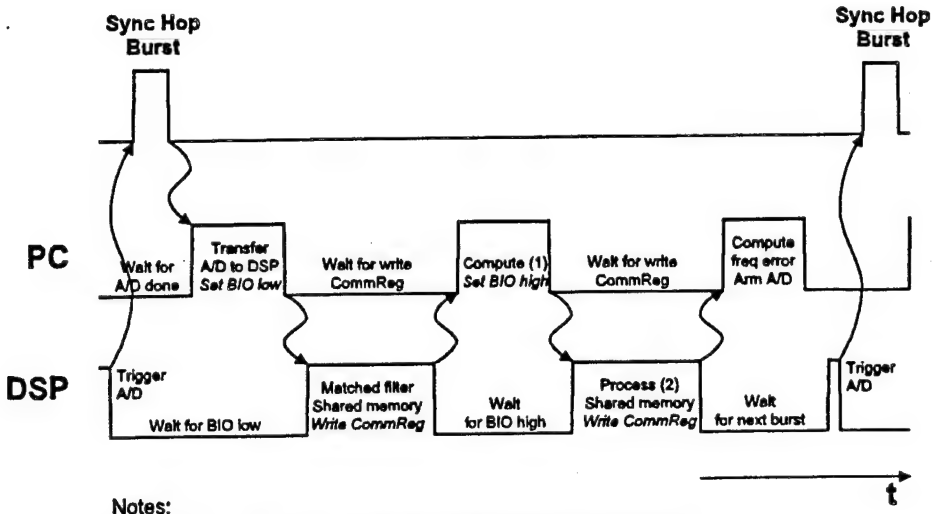
Verification mode begins with the last hop of the first detected sync hop burst and extends to the end of two additional sync hop bursts. The purpose of the verification mode is to make an initial correction to the clock rate and then to bring the clock timing error to an acceptably low value to permit sync hop tracking.

The last hop of the detected sync hop burst is processed by both the envelope detector and quadrature detector paths. The envelope detector signal is processed by the Downlink Synchronization Processor to provide an initial coarse timing estimate of the time-of-arrival of the fourth sync hop. This estimate $\pm 1/3$ hop, is used to reduce the sync hop timing uncertainty to be searched with the quadrature-detected signal.

An estimate is provided using the quadrature-detected data that should be accurate within a half-bit period. The receiver clock phase is modified accordingly, and the DAS 50 is rearmed. Quadrature-detected data for the second sync hop burst is collected and processed. An average burst timing error is computed. The third sync hop burst is subsequently collected and processed, from which a sync hop burst estimate is again obtained. The difference between the timing estimates from the second and third sync hop bursts provides a first approximation of the error in the hop clock rate. The receiver hop clock rate is adjusted accordingly, as well as the hop clock phase. The synchronization process then enters track mode.

F-5 Track Mode

An overview of the handshaking procedure between the Receive Computer and the 'C25 DSP board is provided in Fig. F1. Three traces are shown as a function of time. The top trace represents the reception of a sync hop burst. As earlier discussed, data is collected over nine hops for each sync hop burst. The second trace shows the activity at the Receive Computer (PC): a high level indicating that the PC is busy, and a low level indicates that the PC is waiting for an external action (such as a DSP action). The third trace is of the Downlink Synchronization Processor ('C25 DSP) activity. Once again, a high level indicates busy whereas a low level indicates waiting for external action.



Notes:
(1) Compute in the PC uses raw data from shared memory and
- computes hop timing estimates
- frequency-shifts the raw data
- computes clock rate and phase errors (once per N-burst period)

(2) Process in the DSP uses frequency-shifted data from shared memory and
- matched-filters the data
- adjusts the clock rate and phase (once per N-burst period)

Fig. F1. Overview of synchronization handshaking procedure during track mode.

At the start of a sync hop burst, the DSP is waiting for its BIO line (an external input line) to be set low and the PC is waiting for the DAS 50 A/D board to signal that it has captured the sync hop burst. The PC then reads the A/D data, transfers the data to the DSP, and sets the DSP BIO line low to signal the DSP to proceed with processing the new burst. The PC then waits for the DSP to write to its Communications Register (Comm Reg), signalling the completion of processing. While processing, the DSP computes hop timing error estimate and writes the timing estimate and raw data corresponding to the peak matched filter output, to DSP external memory. The DSP then writes to the Comm Reg and waits for the BIO line to be set high. The PC frequency-shifts the raw data provided by the DSP and computes the hop clock timing and rate error estimates on an N-burst basis. The "N" in N-burst represents the number of sync hop bursts to be included in the timing error and clock rate error estimates. The PC transfers the processed data to DSP external memory, sets the BIO line high and then waits for another write to the Comm Reg. The DSP uses the frequency-shifted data to provide matched filtering on the frequency error estimates and to adjust the clock phase and rate as required. The DSP writes to the Comm Reg and then waits for the BIO line to go low. The PC uses the DSP matched filter data to compute a frequency estimate. The time and frequency error estimates are sent to the Data Logger and are also logged locally on the PC. The PC then arms the DAS 50 A/D board for the next burst and waits for the DAS 50 to indicate that it has collected the specified number of samples. It should be noted that in maintaining the various hop counters, the DSP is able to provide a trigger pulse (to the now armed A/D) that indicates the start of a sync hop burst.

F-6 Clock Rate Adjustments

The bit timing (i.e., clock phase) and clock rate error scenario assumed for the trials is depicted in Fig. F2. A burst timing error estimate, which is obtained from four sync hops, is provided with each sync hop burst. The actual difference in timing error for sync hops in the same burst is assumed to be the same. Timing estimates for a burst will typically be different due to the relatively poor signal-to-noise ratio expected (i.e. Eb/No down to 4 dB). The timing error may however, differ from burst to burst due to, for example, oscillator drift or satellite motion. Consequently, only hops within a burst are averaged to provide a single burst timing estimate. Furthermore the change in burst timing estimate is assumed to be linear over the period that a so-called N-burst estimate is formulated. Typical values of N used for the trials ranged from 8 to 16. The primary trade-off to be considered in selecting the value of N is estimate quality versus signal drift. That is, the timing error estimate improves as the number of sync hop bursts increases; however, the longer one takes to correct the timing, the more severe the clock rate error in terms of bit timing error.

The timing error estimate computed at the end of each N-burst period is used to adjust the clock phase accordingly. The clock rate error however, is applied to an exponentially-weighted, time-averaging filter whose output is used to correct the clock rate. This first order low-pass infinite impulse response (IIR) filter is described by

$$y[n] = \alpha\, x[n] + \beta\, y[n-1]$$

$$\alpha \to 0,\ \beta \to 1 \quad \text{for low corner frequency}$$

where y[n] is the current filtered clock rate error estimate, y[n-1] is the filtered clock rate estimate from the last sync hop burst, x[n] is the clock rate error estimate from the current N-burst and α and ß are filter weights with $\alpha + ß = 1$. A table of α and ß values are provided with the synchronization algorithms to allow the IIR tracking filter corner frequency to be reduced as the estimates become more stable.

The DSP maintains a running average of the magnitude of the sync hop timing error. Estimates which are substantially greater than the average error are discarded. This is done for two reasons: to eliminate estimates associated with the tails of the gaussian distributed random variables and to eliminate poor estimates due to hardware failures such as caused by the Hopping Synthesizer. For the recently completed trials, the threshold for discarding an estimate was based on a factor of three over the average error estimate. Since it is possible to have an average error approaching zero, a minimum, non-zero average was provided. When all four hops within a burst were discarded, the operator was warned by a message which declared a "BAD BURST". This message was also logged by the Receive Computer.

Fig. F2 is a diagram of typical timing error versus time for several N-bursts. The time error starts at 0 at the beginning of the hop. Since the reference clock is not exactly the same as the received timing, there is always an error which increases over time. This is shown by the slope of the line which is steep for a large clock rate error and shallow for a small clock rate error. The time estimates should occur along a line as shown, with the average time error occurring in the middle. At the end of each burst, the clock phase and rate are corrected so the clock rate error should be smaller resulting in more gradual slopes (until limited by noise).

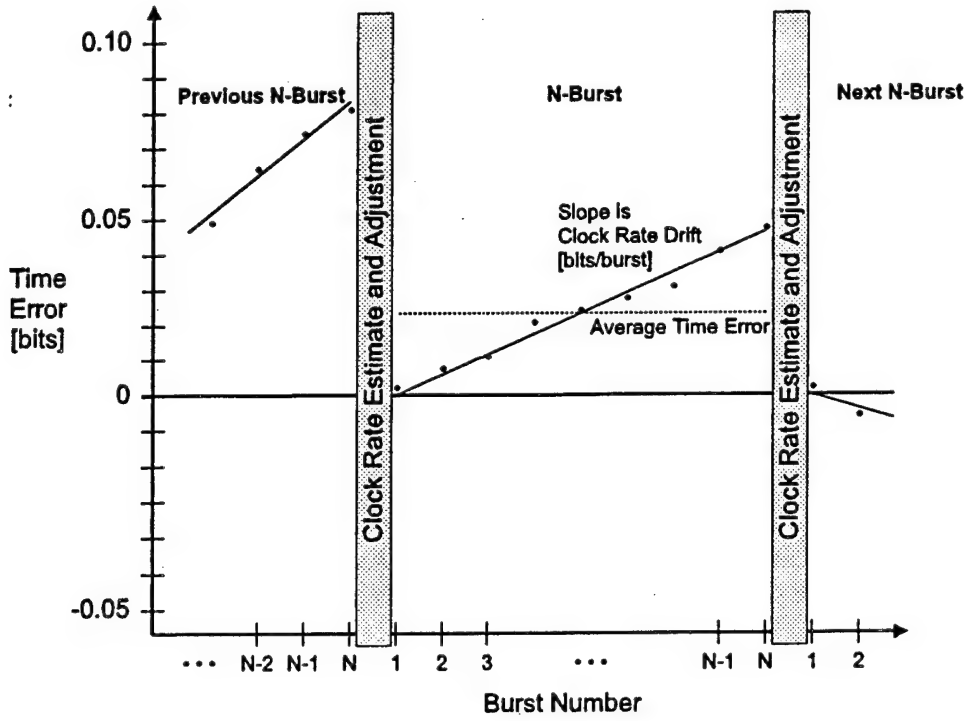


Fig. F2. Typical timing error versus time for N sync hop bursts.

The average time error over an N-burst period based on the individual measurements of each burst is computed using the following equation:

$$\text{Average Time Error} = \frac{1}{N}\sum \text{Time Error}$$

At each N-burst, the average timing error is computed, giving the clock rate drift in following equation:

$$\text{Average Clock Rate Drift} = \frac{1}{N\text{-}1}\sum (\text{Time Error New} - \text{Time Error Old})$$

The N-burst time correction can then be computed from:

$$\text{Time Correction} = -\left(\text{Average Time Error} + \frac{N}{2}\text{Average Clock Rate Drift}\right)$$

Finally, the N-burst clock rate correction is computed, with the results filtered as described previously, before being applied to the clock circuitry:

$$\text{Clock Rate Correction} = \textit{filtered}(\text{Nominal Clock Rate} - \text{Average Clock Rate Drift})$$

Appendix G

Timing and Control Board

This appendix details the Timing and Control Board. The schematic can be found in Fig. G1. This board is connected to the Downlink Synchronization Processor via the DSPLINK. The registers used and their bit fields are detailed below:

Address	Read/Write	Register
10	Write	Hop Number Low Word (16 bits)
11	Write	Hop Number High Word (16 bits)
12	Write	Control/Data D0-D12 DPSK Transmit Data (13 bits): differentially encoded, LSB to be sent first, LSB is DPSK reference bit D13 *not used* D14 Hop Type: 0=sync, 1=data (only used at testpoint) D15 Data Enable: 1 to enable data
13	Write	*wired in, but not used on board*

In Fig. G1 there are several control signals output from the EPROM. The definition of each control signal, corresponding to the control number shown on the diagram, is given below:

Ctl #	Use
1	(not) HClk
2	HClk
3	Coarse A/D Sample Clock
4	2 x Sample/Hold Clock
5	Bit Clock
6	Fine A/D Sample Clock
7	Coarse Integrate/Dump
8	(not) Counter Reset

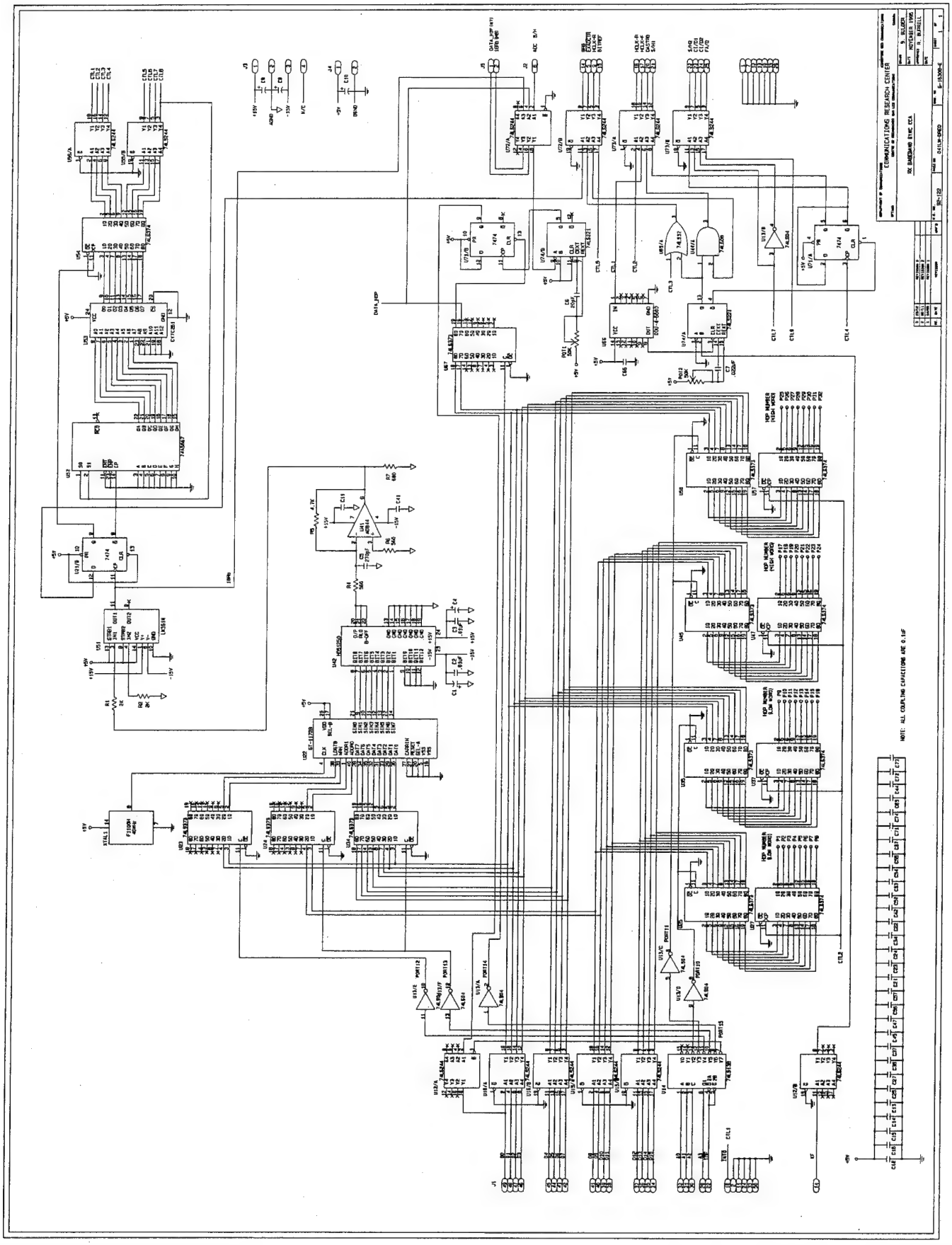


Fig. G1. Timing and Control Board schematic.

Appendix H

Dehopper/Downconverter

This appendix provides the details of the Dehopper/Downconverter. The system diagram can be found in Fig. H1.

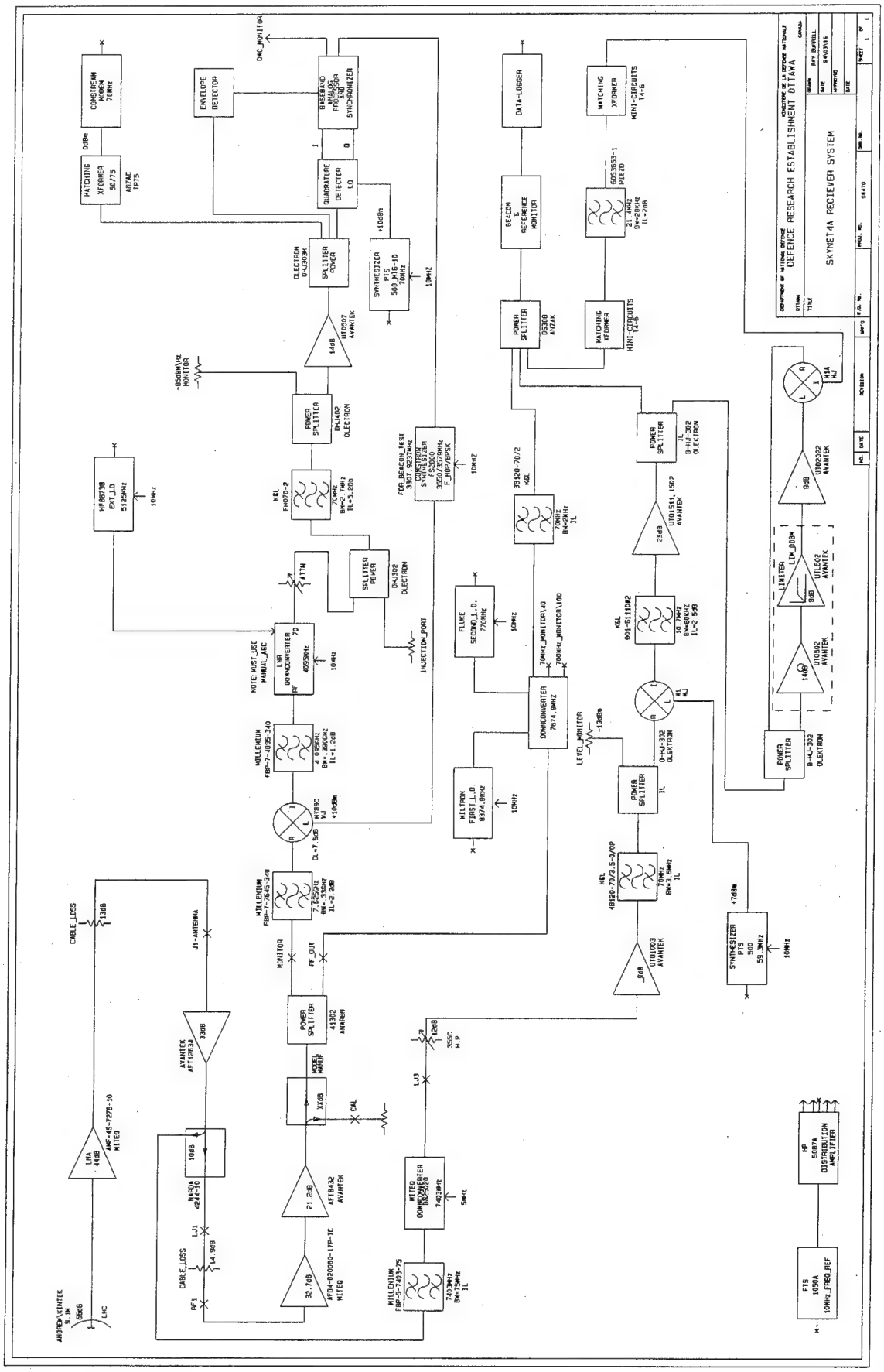


Fig. H1. Dehopper/Downconverter System diagram.

Appendix I

Burst DPSK Demodulator

This appendix provides the details of the Burst DPSK Demodulator. The schematic of the Data Sink and A/D Interface Board can be found in Fig. I1 and Fig. I2. The Burst DPSK Demodulator Analog Board schematic can be found in Fig. I3. The Data Sink and A/D Interface Board is used to interface to a 2.4 kb/s LPC or an HP 1645A Bit-error-rate test set. The other connection is to the Burst DPSK Demodulator Processor through the DSPLINK. The address used on this board is switch selectable to 0, 4, 8, or 12. The DSPLINK registers (for a base address switch setting of 0) and bit fields are detailed below.

Address	Read/Write	Register
0	Read	Receive Data (12 bits): LSB is first bit received
0	Write	Transmit Data (12 bits): LSB is first bit sent
1	Read	Status D0 Hop Rising Edge Latch: 1 after hop clock rising edge (reset after status read) D1 FIFO Not Empty: at least one word ready (reset when FIFO is empty) D3-D11 *not used* D12 Transmit Hold Underflow: 1 = not enough transmit data (reset by write to transmit data) D13 Transmit Hold Empty: 1 = ready for new transmit data (reset by write to transmit data) D14 Receive Data Overflow: 1 = receive data lost because the old data was not read in time (reset by read from receive data) D15 Receive Data Ready: 1 = receive data ready (reset by read from receive data)
1	Write	Command D0 Reset: 1 forces hardware reset (this value is not latched so there is no need to clear it afterwards) D1-D15 *not used*
2	Read	FIFO Data (16 bits)
2	Write	*not used*
3	Read	*not used*
3	Write	*not used*

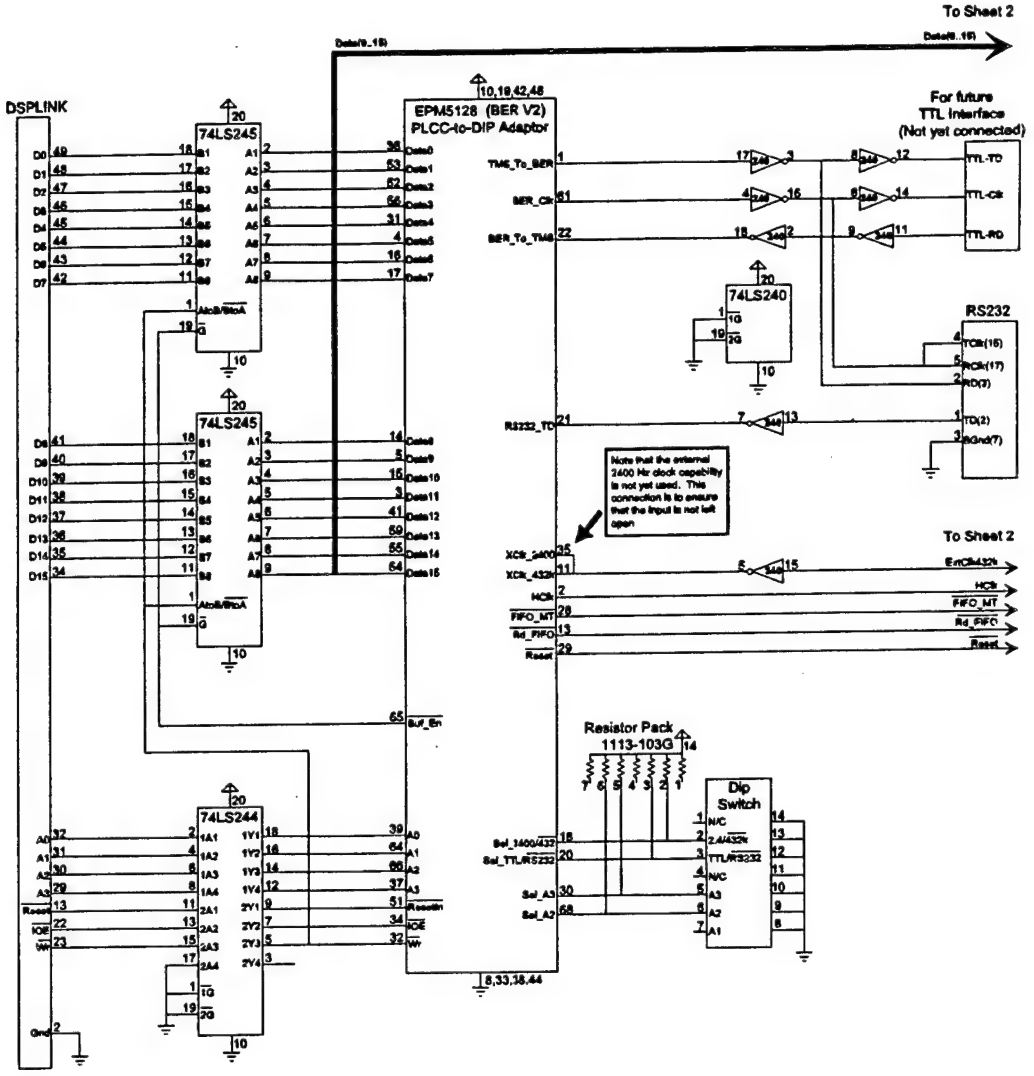


Fig. I1. Data Sink and A/D Interface Board schematic (sheet 1 of 2).

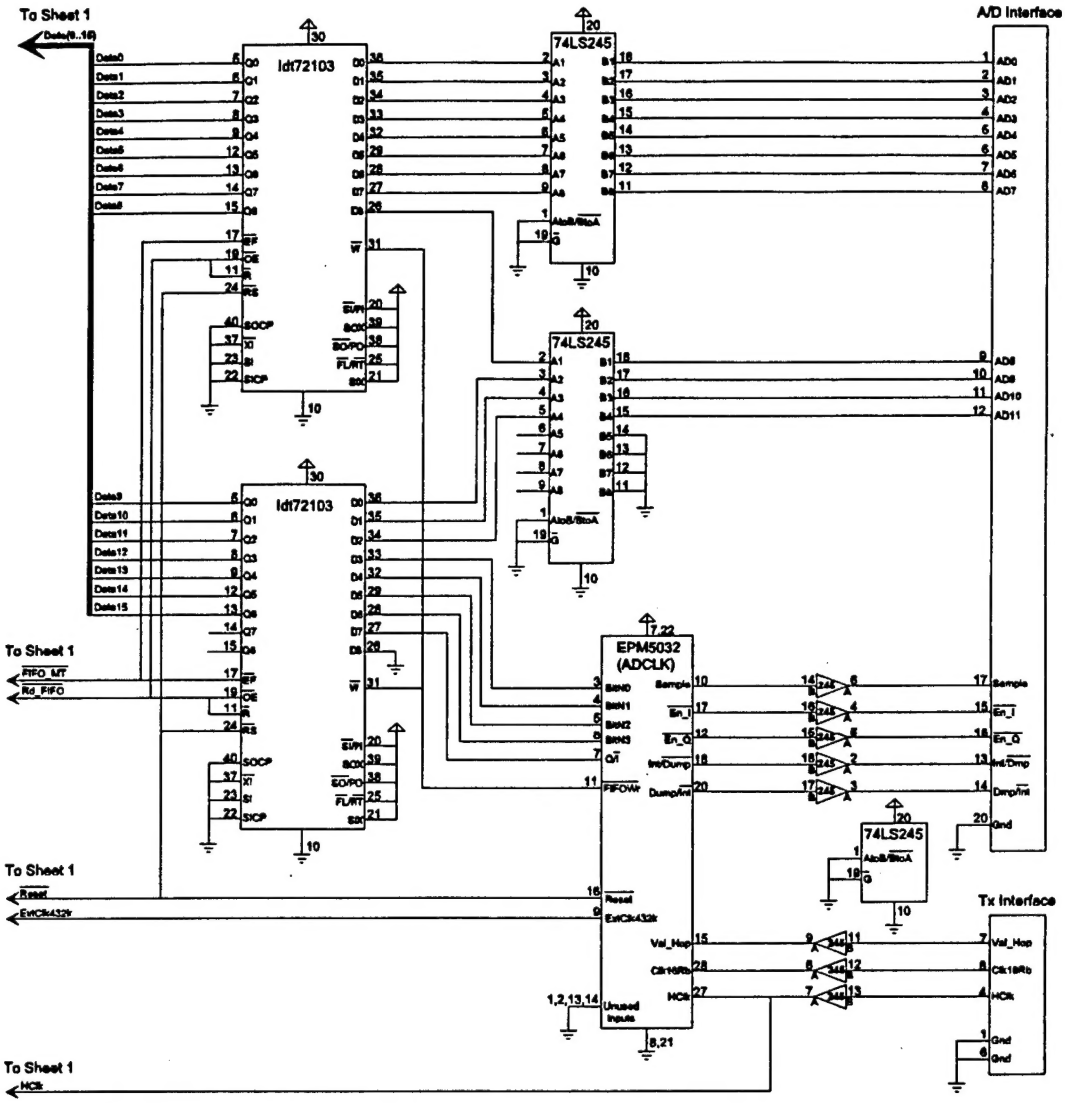


Fig. I2. Data Sink and A/D Interface Board schematic (sheet 2 of 2).

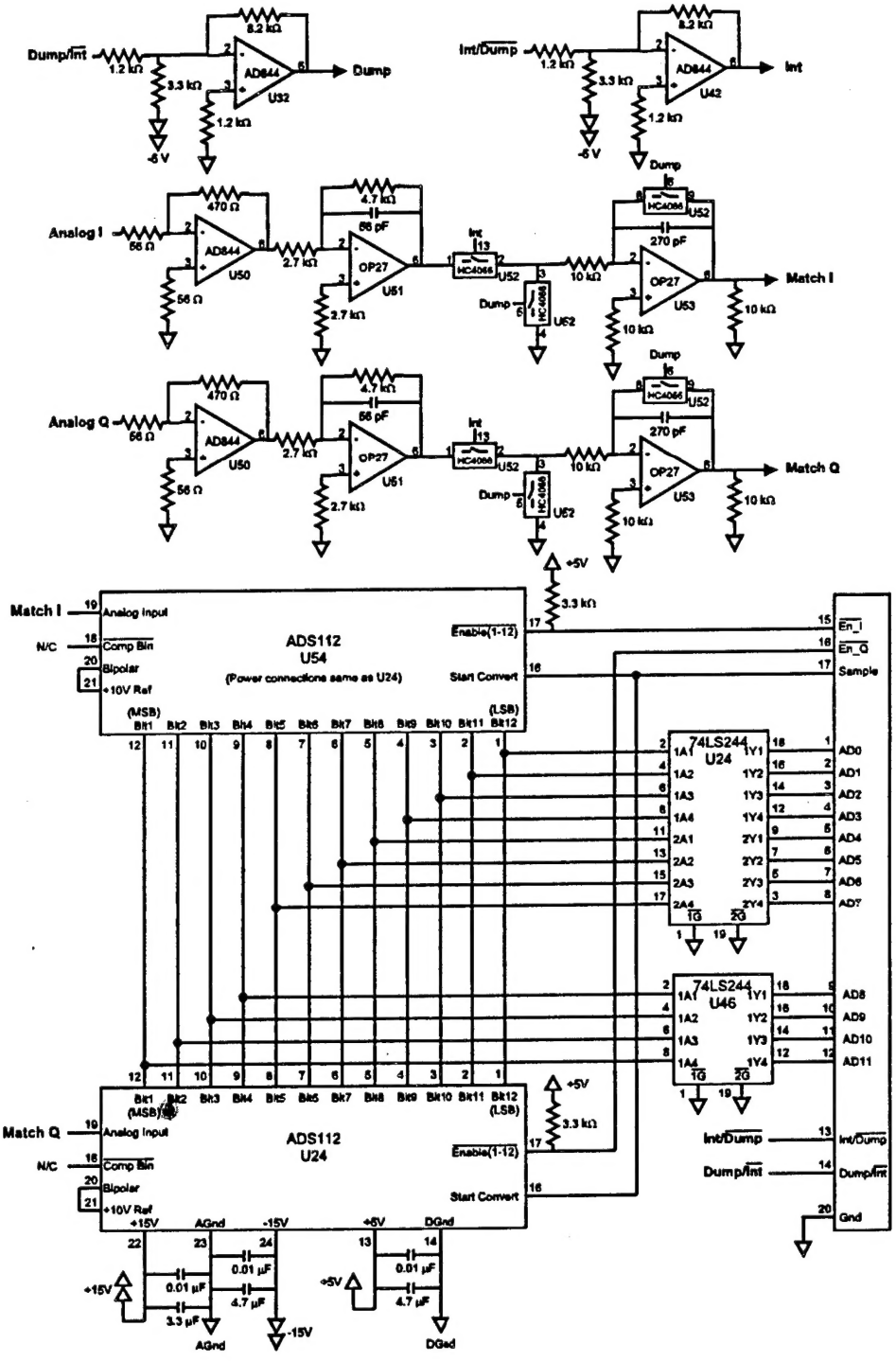


Fig. I3. Burst DPSK Demodulator Analog Board schematic.

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EHF SATCOM offers communications robustness by incorporating wide-band frequency-hopping and on-board satellite processing to mitigate the effects of electronic interference. The same characteristics that make EHF SATCOM robust however, also make it complex. Satellite on-board processing means that synchronization must be achieved for both the uplink and the downlink. The Skynet EHF (extremely high frequency) Downlink Trials consisted of several week-long accesses over Skynet 4A during 1993 and 1994. The whole link (up to satellite and back down) was used to simulate an EHF frequency-hopped downlink from a processing satellite.

To aid in the analysis of EHF SATCOM, in-house ground terminal and payload simulators were developed. For this set of trials, the synchronization and communications aspects of an EHF frequency-hopped downlink using burst differential phase-shift keying modulation were investigated. The payload and ground terminal simulators were developed using a combination of off-the-shelf components and in-house developed hardware and software. The implementation of these two simulators is detailed in this report after the description of the experimental waveform.

The Skynet EHF Downlink Trials were successfully run in week-long experiments over two years. Frequency-hopped spatial and time synchronization were achieved. Data and voice communications were demonstrated with and without time diversity. Problems with the commercial frequency hopping synthesizers precluded the completion of some of the data communications experiments in the time available.

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